cadence

# Allegro PCB Editor Flow – Physical and Spacing Constraints

## Rapid Adoption Kit (RAK)

Product Version 17.4
March 2022

# Contents

# Purpose

The purpose of this RAK is to provide an overview of defining and applying physical and spacing constraints using Constraint Manager in Allegro PCB Editor.

# Audience

This document is intended for PCB designers, hardware designers, and engineers who enter constraints using Constraint Manager.

# Terms

| | |
|---|---|
| CM | Constraint Manager |
| CSet | Constraint Set |
| DP | Differential Pair |
| DRC | Design Rule Check |
| PCSet | Physical Constraint Set |
| SCSet | Spacing Constraint Set |
| Xnet | Extended net |

# Download

RAK testcase database, Scripts and References can be found at ‘Attachments’ and ‘Related Solutions’ sections below the PDF.
This RAK pdf can be searched with the document ‘Title’ on https://support.cadence.com

# Module 1: Physical Constraints

A physical constraint is a rule that characterizes and constrains the physical characteristics of a net. This includes:

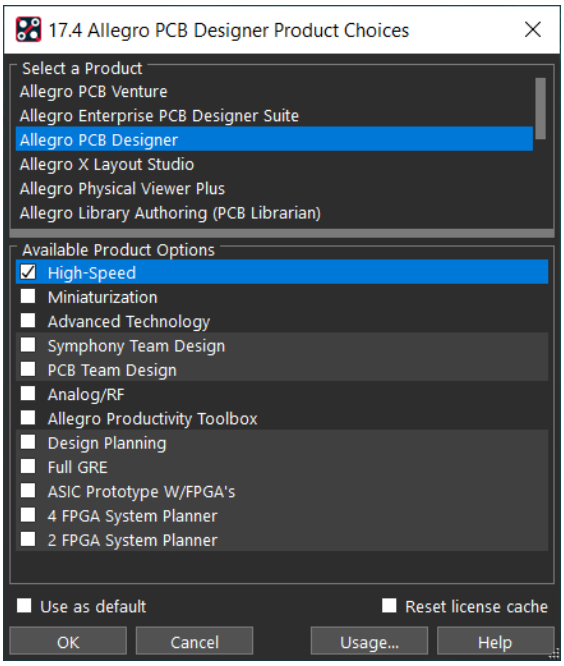
- Trace widths to use in different areas and on different layers
- Allowable connections on a layer
- Acceptable vias to use on a net
- By-layer differential pair constraints

Physical constraints can be applied at the Xnet and Net levels.

All designs begin with a default constraint set in the Physical and Spacing domains. The default CSet cannot be deleted. Also, you cannot remove any values from within it. These values can be modified though. The labs in this document outline how to create and assign Physical and Spacing CSets to create exceptions to the default CSet.

The design used in these labs is a processor-based design with two DDR4 banks (DDR4_BANK0 and DDR4_BANK1). Each bank is defined as a net group that contains two net groups – one for address/command/control (DDR4_BANKx_ADD) and another for data (DDR4_BANKx_DATA).

## Lab 1: Setting Default Physical Constraints

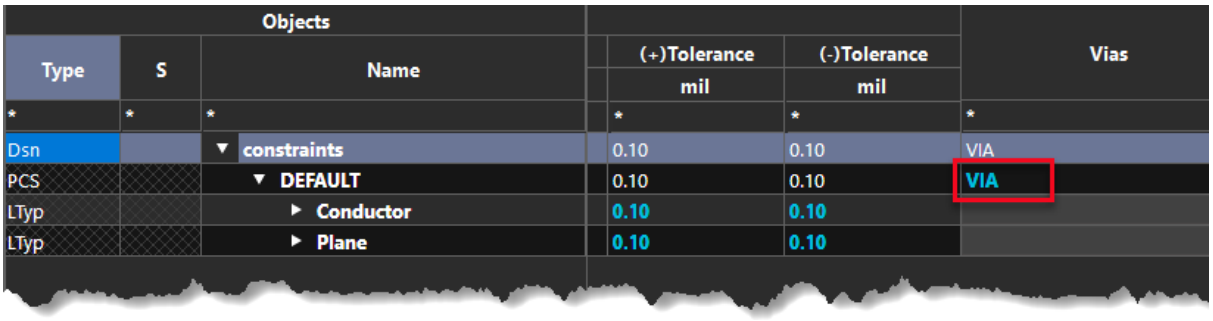


2. Select **Setup > Constraints > Physical** to open CM in the Physical domain.

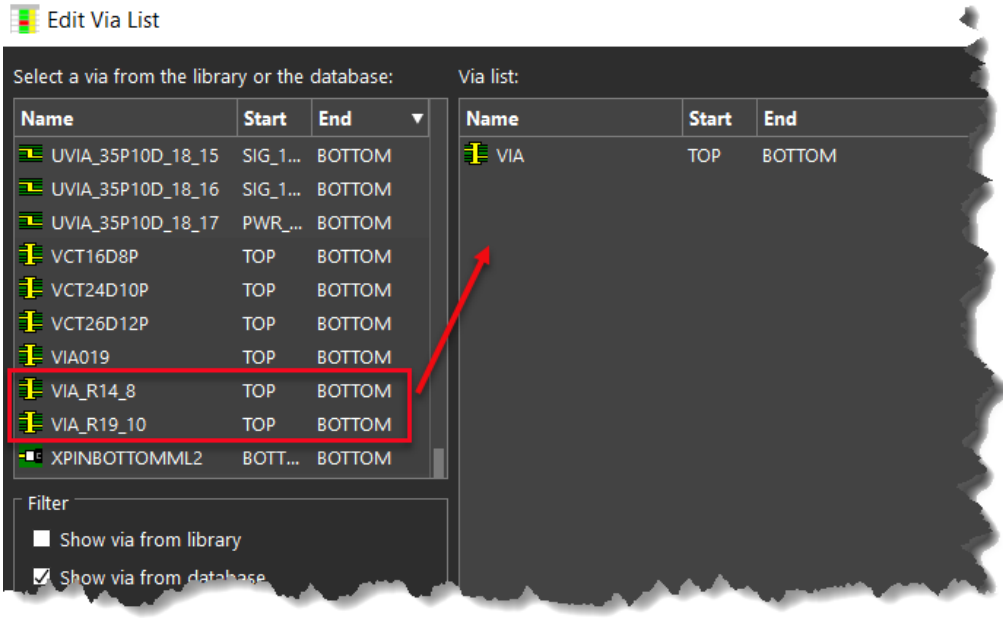
   The first step in creating physical rules is to set the default rules. These rules will be used for the nets that have no special routing requirements.

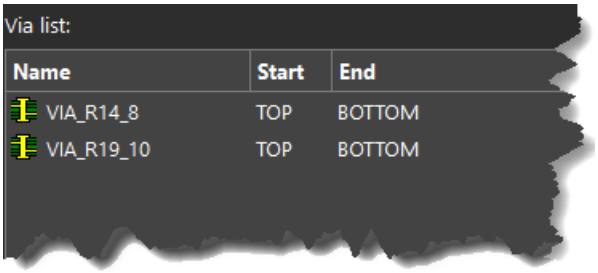
3. Select the **Physical Constraint Set > All Layers** worksheet. A DEFAULT PCSet has been defined.

| Objects | | | Line Width | | Neck | | Differential Pair | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Type | S | Name | Min | Max | Min Width | Max Length | Min Line Spacing | Primary Gap | Neck Gap | (+)Tolerance | (-)Tolerance |
| | | | mil | mil | mil | mil | mil | mil | mil | mil | mil |
| * | * | * | * | * | * | * | * | * | * | * | * |
| Dsn | | constraints | 5.00 | 40.00 | 5.00 | 0.00 | 4.00 | 5.00 | 0.00 | 0.10 | 0.10 |
| PCS | | DEFAULT | 5.00 | 40.00 | 5.00 | 0.00 | 4.00 | 5.00 | 0.00 | 0.10 | 0.10 |
| LTyp | | Conductor | 5.00 | 40.00 | 5.00 | 0.00 | 4.00 | 5.00 | 0.00 | 0.10 | 0.10 |
| LTyp | | Plane | 5.00 | 40.00 | 5.00 | 0.00 | 4.00 | 5.00 | 0.00 | 0.10 | 0.10 |



| Objects | | | | | |
|---|---|---|---|---|---|
| Type | S | Name | (+)Tolerance | (-)Tolerance | Vias |
| | | | mil | mil | |
| * | * | * | * | * | * |
| Dsn | | constraints | 0.10 | 0.10 | VIA |
| PCS | | DEFAULT | 0.10 | 0.10 | VIA |
| LTyp | | Conductor | 0.10 | 0.10 | |
| LTyp | | Plane | 0.10 | 0.10 | |

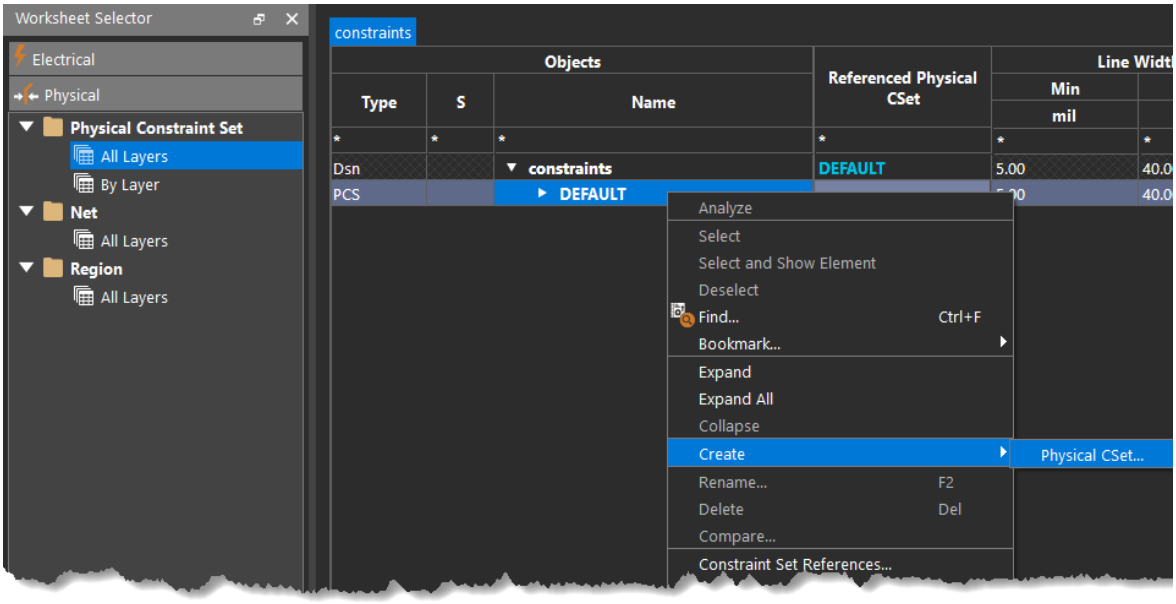


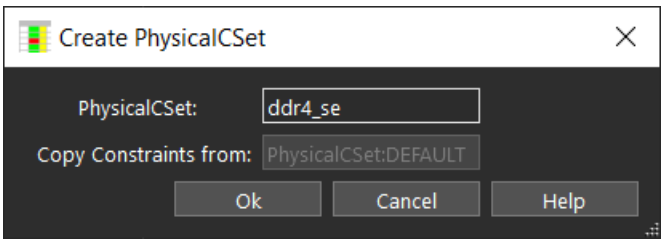



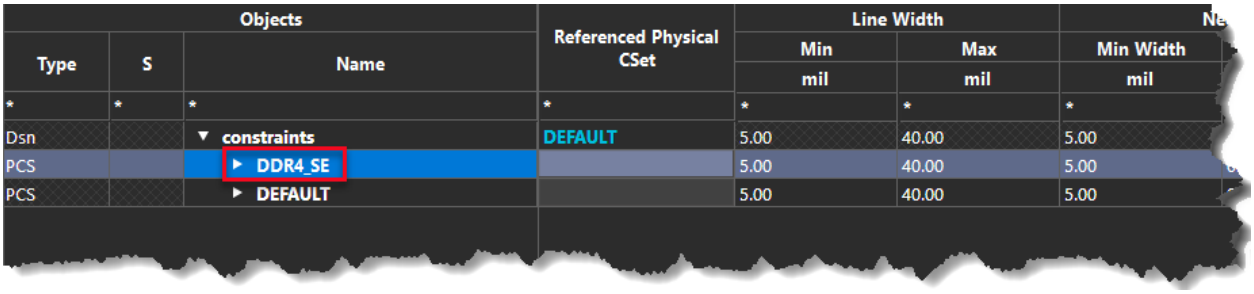

| Objects | | | | | |
|---|---|---|---|---|---|
| Type | S | Name | (+)Tolerance mil | (-)Tolerance mil | Vias |
| * | * | * | * | * | * |
| Dsn | | constraints | 0.10 | 0.10 | VIA_R14_8:VIA_R19_10 |
| PCS | | DEFAULT | 0.10 | 0.10 | VIA_R14_8:VIA_R19_10 |
| LTyp | | Conductor | 0.10 | 0.10 | |
| LTyp | | Plane | 0.10 | 0.10 | |

## Lab 2: Defining a New Physical Constraint Set

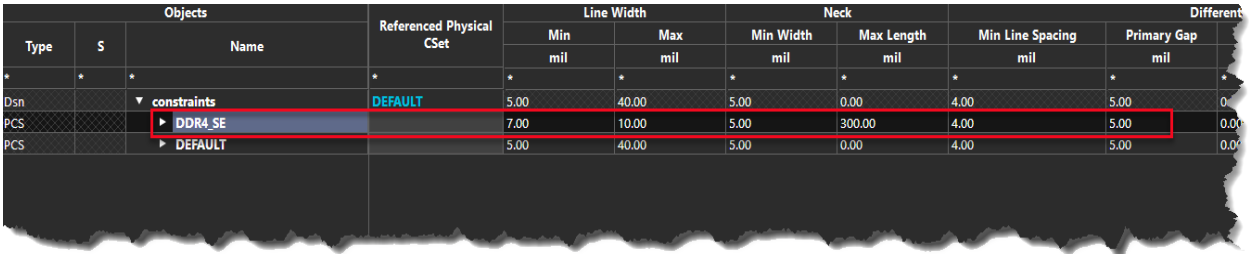
You will probably have nets that require different physical rules than the default rules. New PCSets need to be created for these nets. You can create as many PCSets as required in your design.





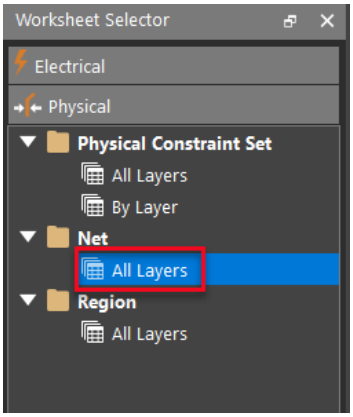
| Objects | | | Referenced Physical CSet | Line Width | | Ne |
|---|---|---|---|---|---|---|
| Type | S | Name | | Min | Max | Min Width |
| | | | | mil | mil | mil |
| * | * | * | * | * | * | * |
| Dsn | | constraints | DEFAULT | 5.00 | 40.00 | 5.00 |
| PCS | | DDR4_SE | | 5.00 | 40.00 | 5.00 |
| PCS | | DEFAULT | | 5.00 | 40.00 | 5.00 |



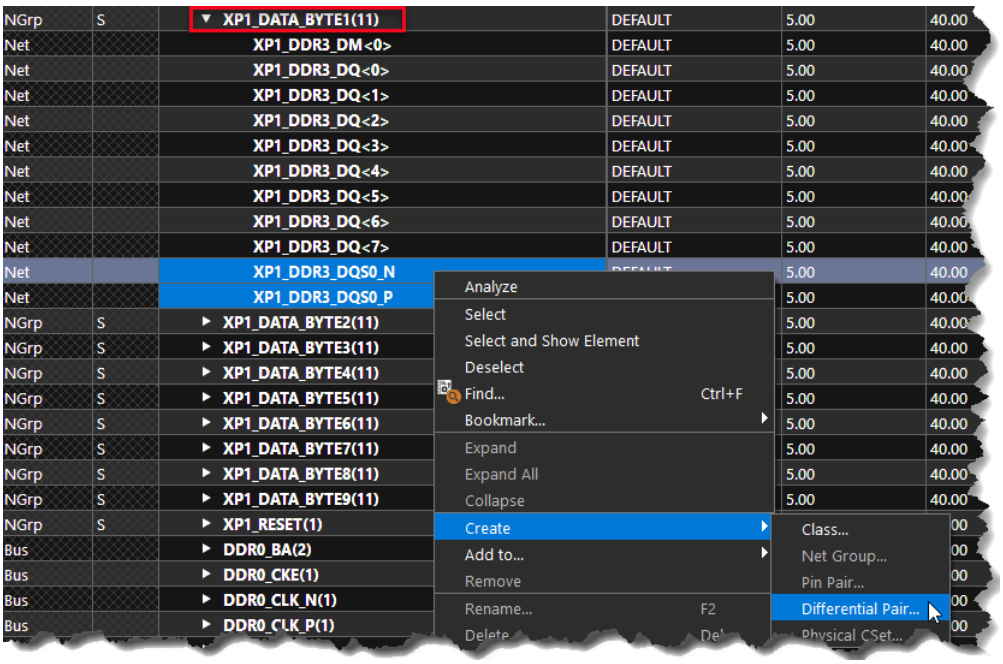
| Objects | | | Referenced Physical CSet | Line Width | | Neck | | Different | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Type | S | Name | | Min | Max | Min Width | Max Length | Min Line Spacing | Primary Gap | |
| | | | | mil | mil | mil | mil | mil | mil | |
| * | * | * | * | * | * | * | * | * | * | * |
| Dsn | | constraints | DEFAULT | 5.00 | 40.00 | 5.00 | 0.00 | 4.00 | 5.00 | 0 |
| PCS | | DDR4_SE | | 7.00 | 10.00 | 5.00 | 300.00 | 4.00 | 5.00 | 0.0 |
| PCS | | DEFAULT | | 5.00 | 40.00 | 5.00 | 0.00 | 4.00 | 5.00 | 0.0 |

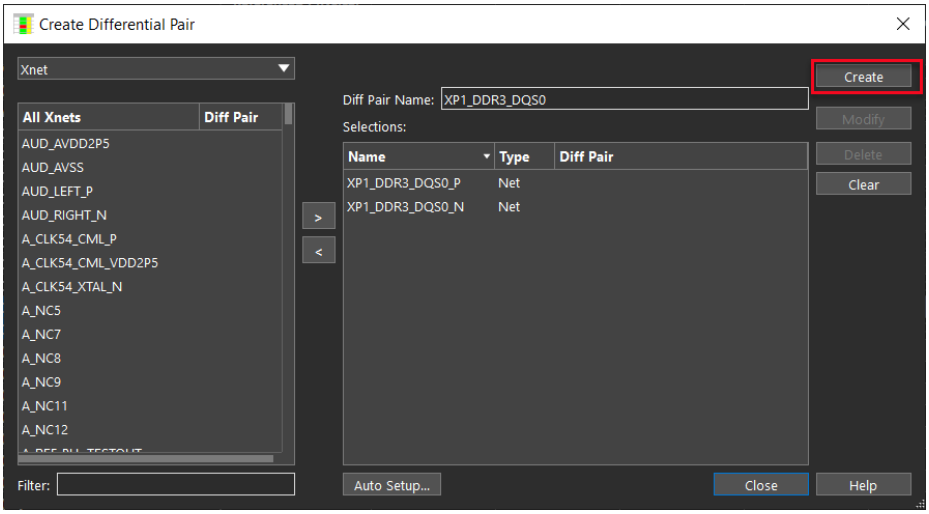
## Lab 3: Defining Differential Pairs

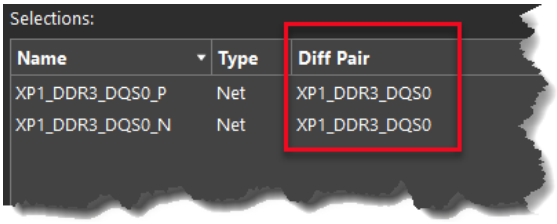
This lab will outline several ways to create differential pairs in CM.



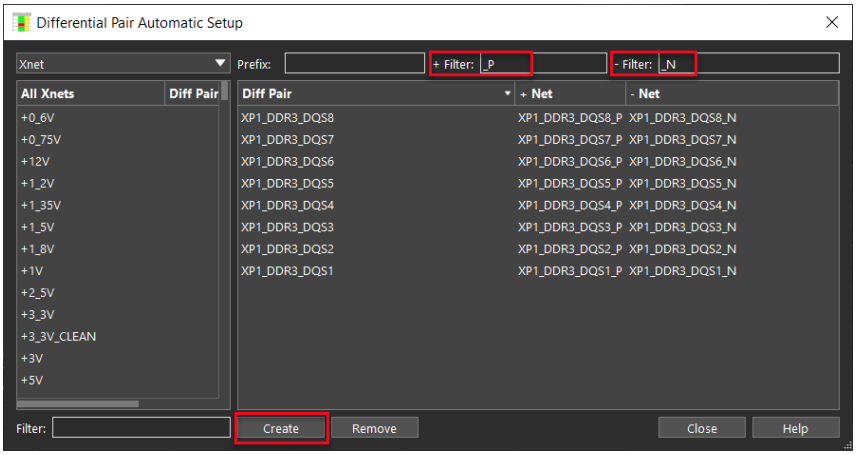

2. Expand the **XP1_DATA_BYTE1** Net Group (NGrp).
3. Select the **XP1_DDR3_DQS0_N** and **XP1_DDR3_DQS0_P** nets.





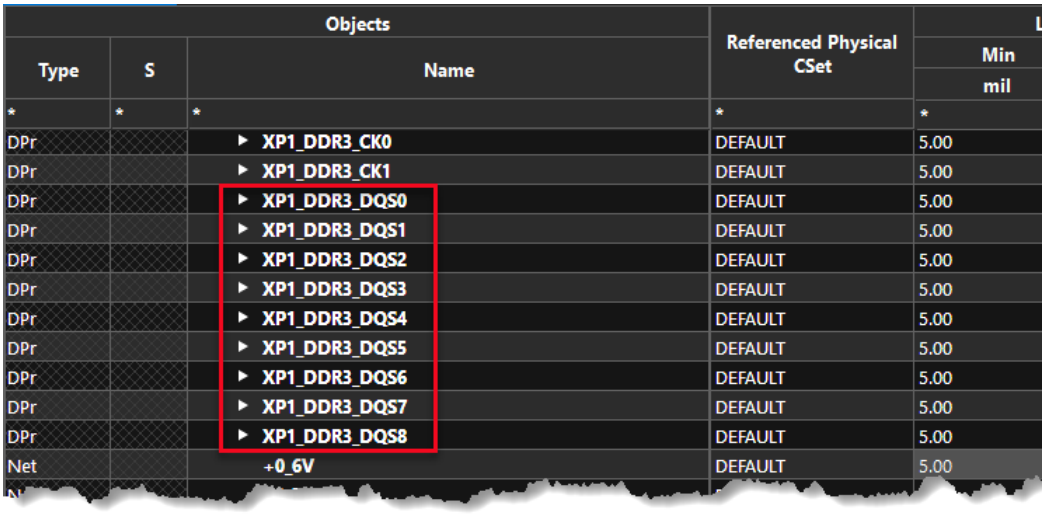




6. Diff pairs can also be created automatically based on naming conventions. Select **Auto Setup** in the **Create Differential Pair** form.



8. Click **Create** to create the differential pairs.

9. Close the Differential Pair Automatic Setup and Create Differential Pair forms.



| Objects | | | Referenced Physical CSet | Min mil |
|---|---|---|---|---|
| Type | S | Name | | |
| * | * | * | * | * |
| DPr | | XP1_DDR3_CK0 | DEFAULT | 5.00 |
| DPr | | XP1_DDR3_CK1 | DEFAULT | 5.00 |
| DPr | | XP1_DDR3_DQS0 | DEFAULT | 5.00 |
| DPr | | XP1_DDR3_DQS1 | DEFAULT | 5.00 |
| DPr | | XP1_DDR3_DQS2 | DEFAULT | 5.00 |
| DPr | | XP1_DDR3_DQS3 | DEFAULT | 5.00 |
| DPr | | XP1_DDR3_DQS4 | DEFAULT | 5.00 |
| DPr | | XP1_DDR3_DQS5 | DEFAULT | 5.00 |
| DPr | | XP1_DDR3_DQS6 | DEFAULT | 5.00 |
| DPr | | XP1_DDR3_DQS7 | DEFAULT | 5.00 |
| DPr | | XP1_DDR3_DQS8 | DEFAULT | 5.00 |
| Net | | +0_6V | DEFAULT | 5.00 |

## Lab 4: Defining Differential Pair Constraints by Layer

To maintain the required impedance, different line width and spacing can be defined for different layers. This lab will demonstrate how to create a PCSet for differential pairs where the spacing and line width is different on the inner and outer layers.

1. In the Physical domain of CM, select the **Physical Constraint Set > All Layers** worksheet.

2. Select **Objects > Create > Physical CSet** from the CM menu.

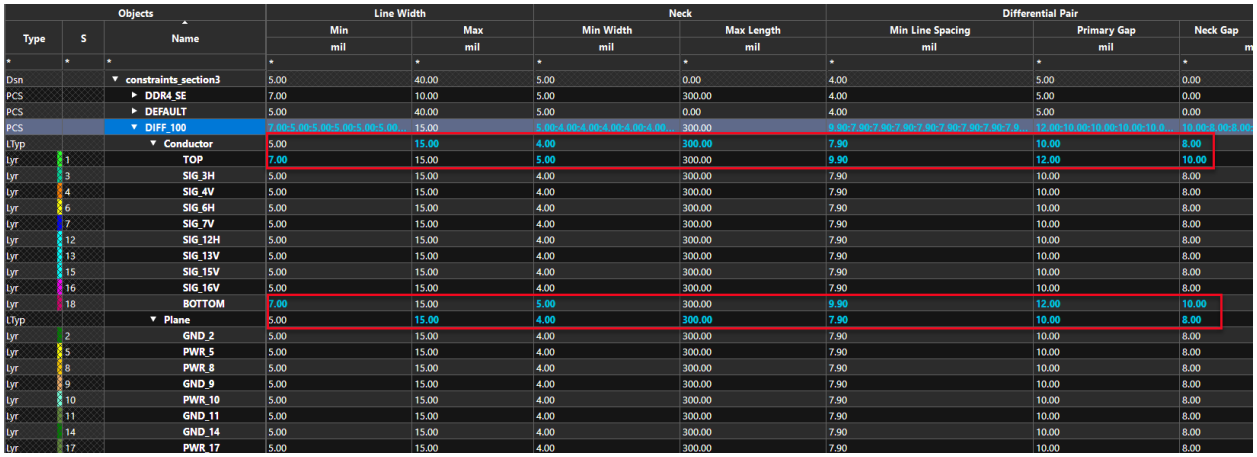
3. Name the PCSet **DIFF_100** and click **Ok**.

4. Expand the **DIFF_100** PCSet, then expand the Conductor and Plane layer types to view layers beneath each.

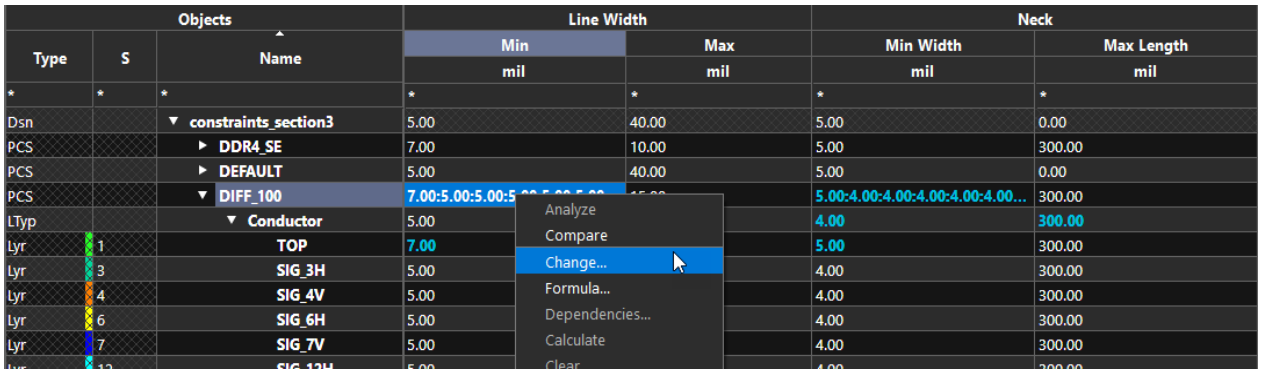
5. Change the following constraints (you will need to change the Primary Gap prior to changing the Min Line Spacing):

| | |
|---|---|
| **Min Line Width** | 5 |
| **Max Line Width** | 15 |
| **Min Neck Width** | 4 |
| **Max Neck Length** | 300 |
| **Primary Gap** | 10 |

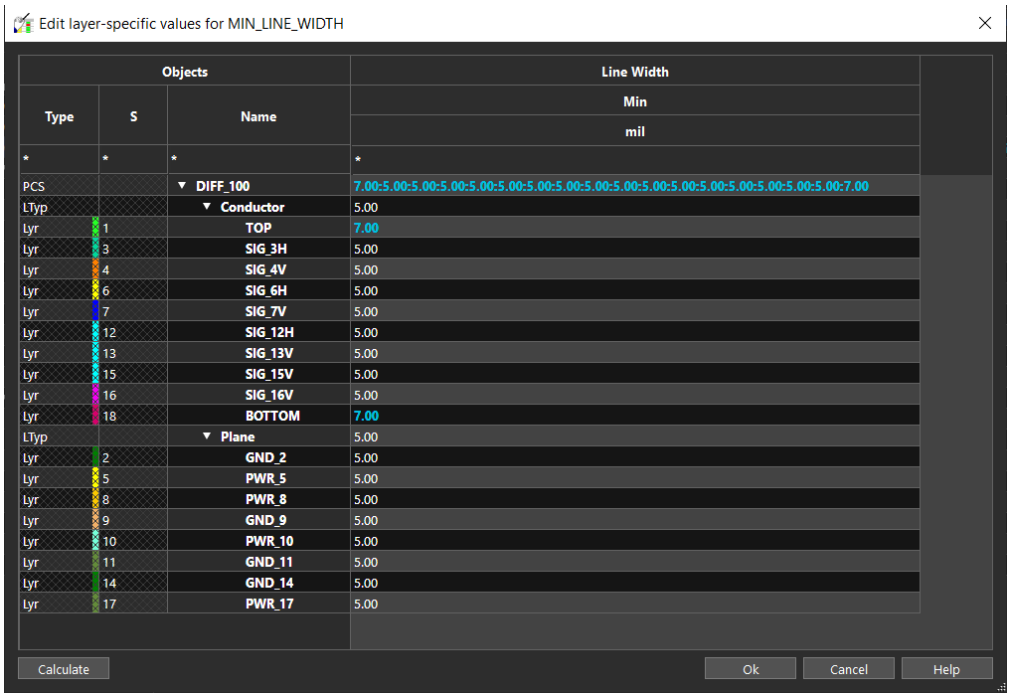
**DP Neck Gap** 8
**Min Line Spacing** 7.9



| Objects | | | Line Width | | Neck | | Differential Pair | | |
|---|---|---|---|---|---|---|---|---|---|
| Type | S | Name | Min | Max | Min Width | Max Length | Min Line Spacing | Primary Gap | Neck Gap |
| | | | mil | mil | mil | mil | mil | mil | m |
| * | * | * | * | * | * | * | * | * | * |
| Dsn | | constraints_section3 | 5.00 | 40.00 | 5.00 | 0.00 | 4.00 | 5.00 | 0.00 |
| PCS | | DDR4_SE | 7.00 | 10.00 | 5.00 | 300.00 | 4.00 | 5.00 | 0.00 |
| PCS | | DEFAULT | 5.00 | 40.00 | 5.00 | 0.00 | 4.00 | 5.00 | 0.00 |
| PCS | | DIFF_100 | 7.00:5.00:5.00:5.00:5.00... | 15.00 | 5.00:4.00:4.00:4.00:4.00:4.00... | 300.00 | 9.90:7.90:7.90:7.90:7.90:7.90:7.90:7.9... | 12.00:10.00:10.00:10.00:10.00:10.0... | 10.00:8.00:8.00 |
| LTyp | | Conductor | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 1 | TOP | 7.00 | 15.00 | 5.00 | 300.00 | 9.90 | 12.00 | 10.00 |
| Lyr | 3 | SIG_3H | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 4 | SIG_4V | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 6 | SIG_6H | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 7 | SIG_7V | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 12 | SIG_12H | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 13 | SIG_13V | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 15 | SIG_15V | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 16 | SIG_16V | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 18 | BOTTOM | 7.00 | 15.00 | 5.00 | 300.00 | 9.90 | 12.00 | 10.00 |
| LTyp | | Plane | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 2 | GND_2 | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 5 | PWR_5 | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 8 | PWR_8 | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 9 | GND_9 | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 10 | PWR_10 | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 11 | GND_11 | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 14 | GND_14 | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |
| Lyr | 17 | PWR_17 | 5.00 | 15.00 | 4.00 | 300.00 | 7.90 | 10.00 | 8.00 |

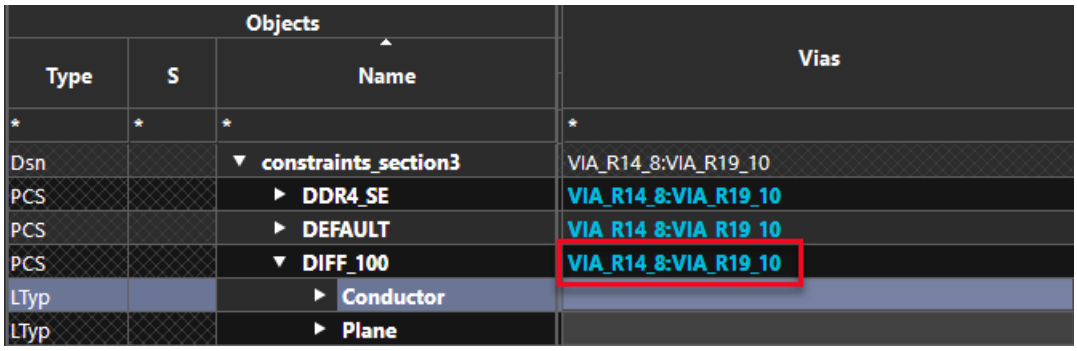


| Objects | | | Line Width | | Neck | |
|---|---|---|---|---|---|---|
| Type | S | Name | Min | Max | Min Width | Max Length |
| | | | mil | mil | mil | mil |
| * | * | * | * | * | * | * |
| Dsn | | constraints_section3 | 5.00 | 40.00 | 5.00 | 0.00 |
| PCS | | DDR4_SE | 7.00 | 10.00 | 5.00 | 300.00 |
| PCS | | DEFAULT | 5.00 | 40.00 | 5.00 | 0.00 |
| PCS | | DIFF_100 | 7.00:5.00:5.00:5 | | 5.00:4.00:4.00:4.00:4.00:4.00... | 300.00 |
| LTyp | | Conductor | 5.00 | | 4.00 | 300.00 |
| Lyr | 1 | TOP | 7.00 | | 5.00 | 300.00 |
| Lyr | 3 | SIG_3H | 5.00 | | 4.00 | 300.00 |
| Lyr | 4 | SIG_4V | 5.00 | | 4.00 | 300.00 |
| Lyr | 6 | SIG_6H | 5.00 | | 4.00 | 300.00 |
| Lyr | 7 | SIG_7V | 5.00 | | 4.00 | 300.00 |



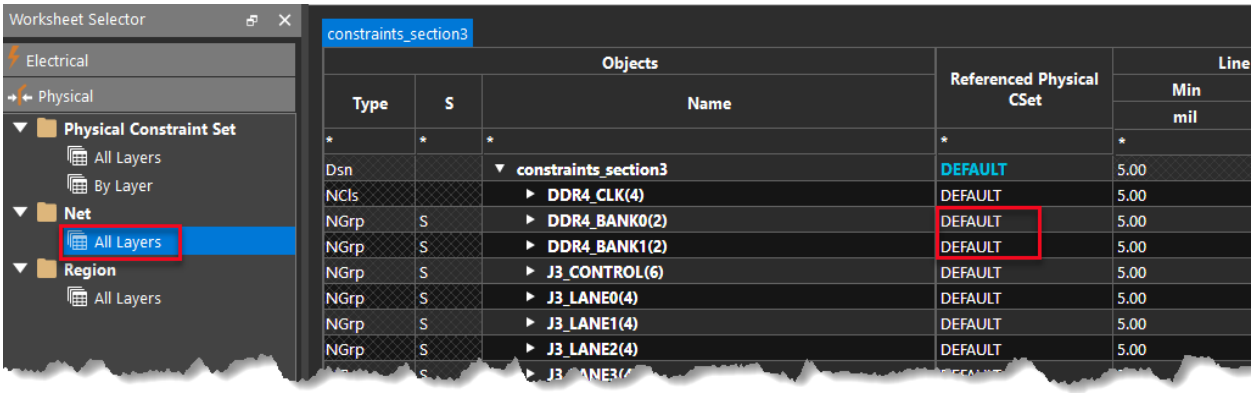

8. Select **Cancel** to close the form.

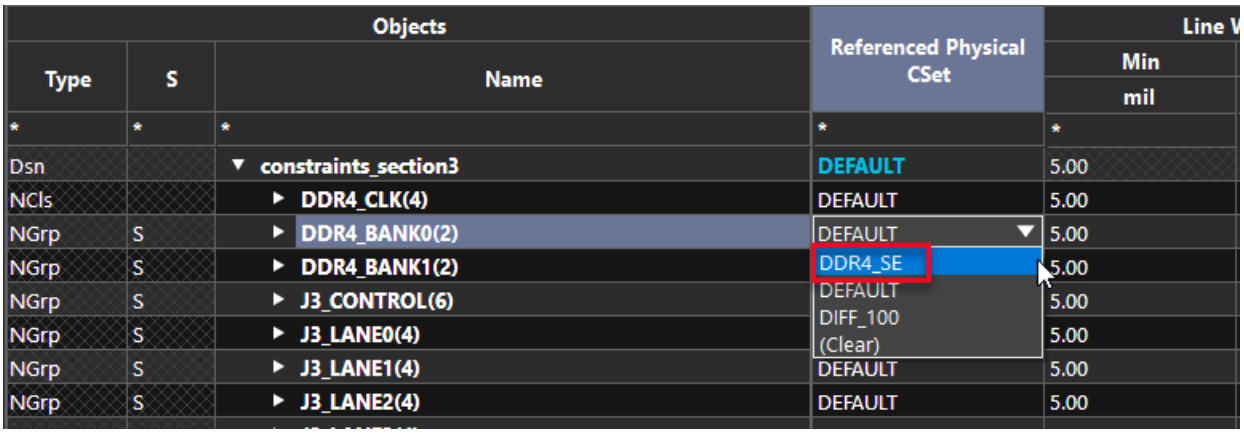
9. If necessary, add **VIA_R14_8** and **VIA_R19_10** to the Via list.

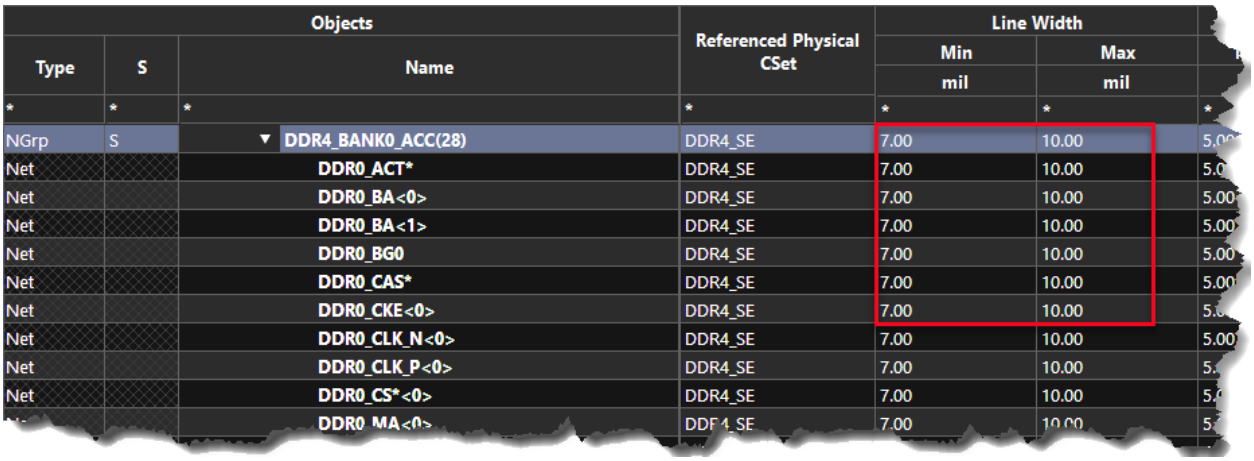


## Lab 5: Assigning Physical Constraint Sets

Once the constraint sets are defined, they need to be assigned to nets in the design.



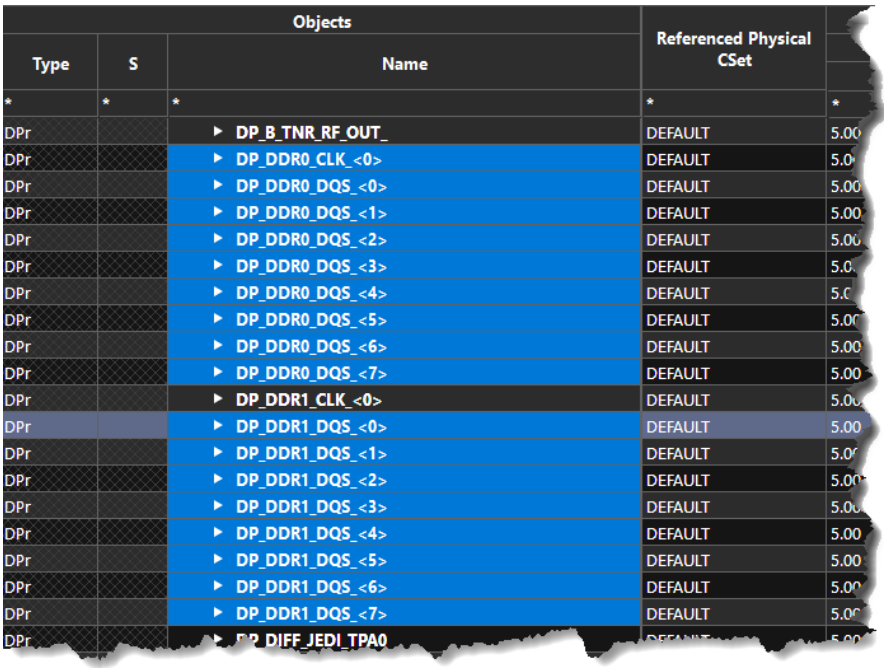





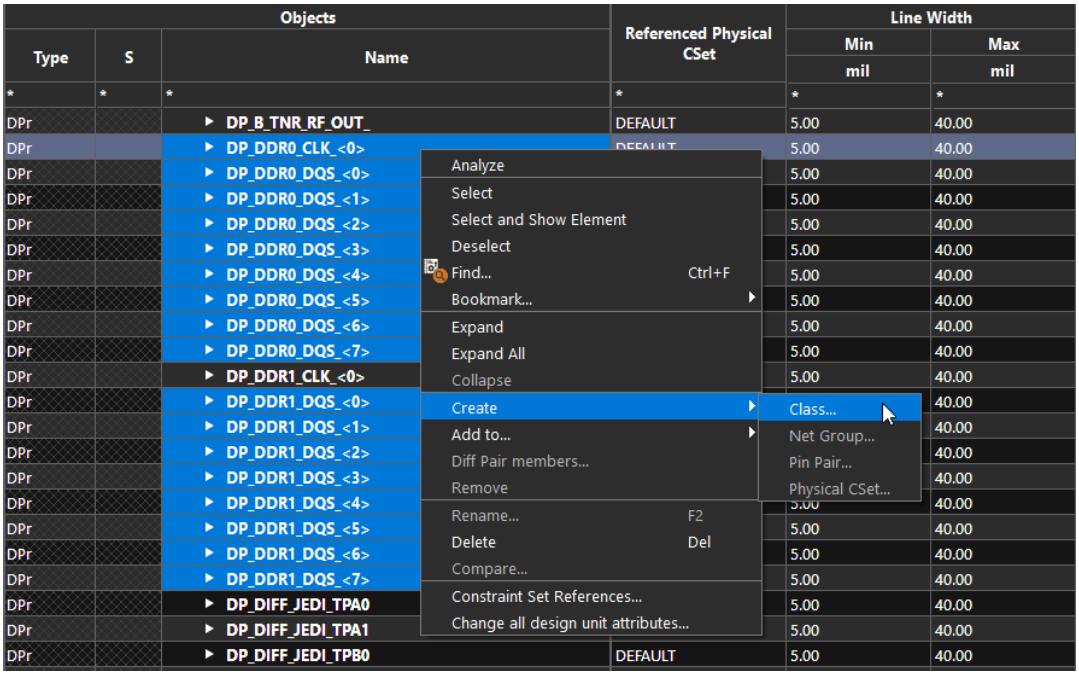
| Objects | | | Referenced Physical CSet | Line Width | |
|---|---|---|---|---|---|
| Type | S | Name | | Min | Max |
| | | | | mil | mil |
| * | * | * | * | * | * |
| NGrp | S | DDR4_BANK0_ACC(28) | DDR4_SE | 7.00 | 10.00 |
| Net | | DDR0_ACT* | DDR4_SE | 7.00 | 10.00 |
| Net | | DDR0_BA<0> | DDR4_SE | 7.00 | 10.00 |
| Net | | DDR0_BA<1> | DDR4_SE | 7.00 | 10.00 |
| Net | | DDR0_BG0 | DDR4_SE | 7.00 | 10.00 |
| Net | | DDR0_CAS* | DDR4_SE | 7.00 | 10.00 |
| Net | | DDR0_CKE<0> | DDR4_SE | 7.00 | 10.00 |
| Net | | DDR0_CLK_N<0> | DDR4_SE | 7.00 | 10.00 |
| Net | | DDR0_CLK_P<0> | DDR4_SE | 7.00 | 10.00 |
| Net | | DDR0_CS*<0> | DDR4_SE | 7.00 | 10.00 |
| | | DDR0_MA<0> | DDR4_SE | 7.00 | 10.00 |

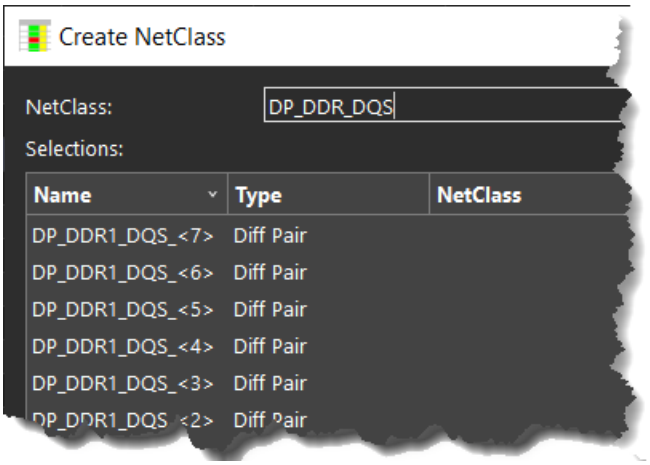
The DDR strobe differential pairs (DP_DDRx_DQS) can be included in a single net class, allowing for easier application of the DIFF_100 PCSet.

4. Scroll down to the differential pair (DPr) objects in the **Net > All Layers** worksheet.

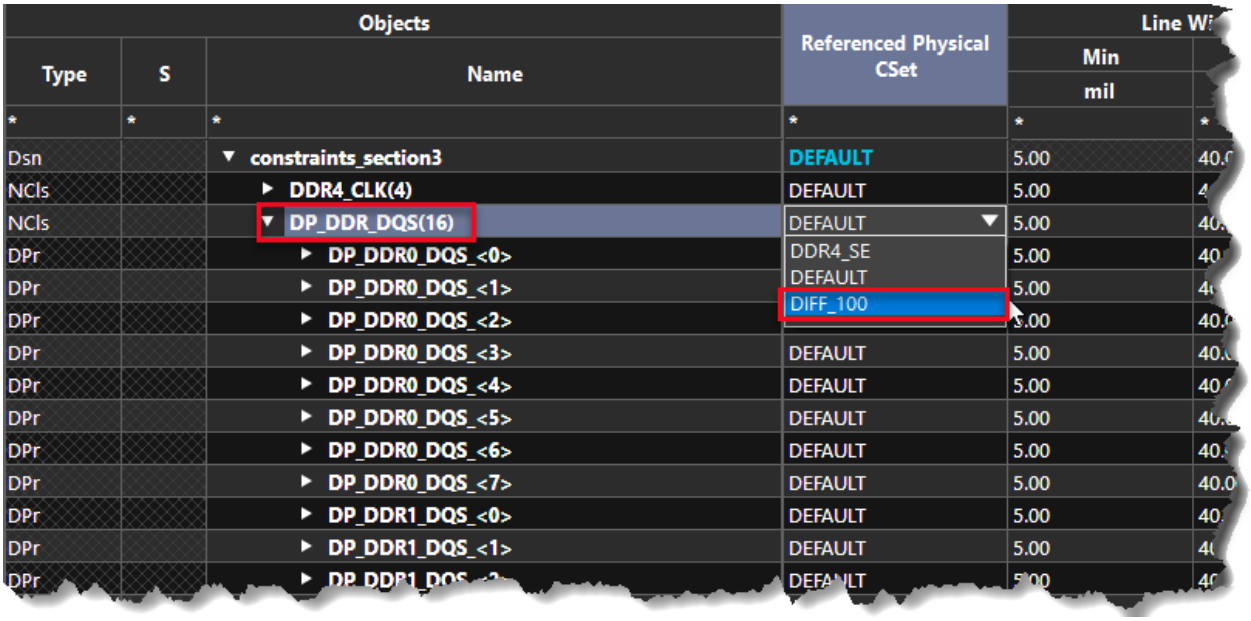


| Objects | | | Referenced Physical CSet | |
|---|---|---|---|---|
| Type | S | Name | | |
| * | * | * | * | * |
| DPr | | DP_B_TNR_RF_OUT_ | DEFAULT | 5.00 |
| DPr | | DP_DDR0_CLK_<0> | DEFAULT | 5.0 |
| DPr | | DP_DDR0_DQS_<0> | DEFAULT | 5.00 |
| DPr | | DP_DDR0_DQS_<1> | DEFAULT | 5.00 |
| DPr | | DP_DDR0_DQS_<2> | DEFAULT | 5.00 |
| DPr | | DP_DDR0_DQS_<3> | DEFAULT | 5.0 |
| DPr | | DP_DDR0_DQS_<4> | DEFAULT | 5.0 |
| DPr | | DP_DDR0_DQS_<5> | DEFAULT | 5.00 |
| DPr | | DP_DDR0_DQS_<6> | DEFAULT | 5.00 |
| DPr | | DP_DDR0_DQS_<7> | DEFAULT | 5.00 |
| DPr | | DP_DDR1_CLK_<0> | DEFAULT | 5.00 |
| DPr | | DP_DDR1_DQS_<0> | DEFAULT | 5.00 |
| DPr | | DP_DDR1_DQS_<1> | DEFAULT | 5.0 |
| DPr | | DP_DDR1_DQS_<2> | DEFAULT | 5.00 |
| DPr | | DP_DDR1_DQS_<3> | DEFAULT | 5.00 |
| DPr | | DP_DDR1_DQS_<4> | DEFAULT | 5.00 |
| DPr | | DP_DDR1_DQS_<5> | DEFAULT | 5.00 |
| DPr | | DP_DDR1_DQS_<6> | DEFAULT | 5.00 |
| DPr | | DP_DDR1_DQS_<7> | DEFAULT | 5.00 |
| DPr | | DP_DIFF_JEDI_TPA0 | | |




8. Scroll to the top of the worksheet to see the **DP_DDR_DQS** net class (NCls).



# Module 2: Spacing Constraints

A spacing constraint is a rule that specifies the spacing between two physical objects. These objects are the physical instantiation of different nets. Spacing constraints apply to both Xnet level and Net level. Line-to-line spacing is an example of a spacing constraint that applies between the two nets.

The default SCSet in this design uses 5-mil spacing clearances, but the design requires 8-mil spacing.

## Lab 6: Defining a New Spacing Constraint Set

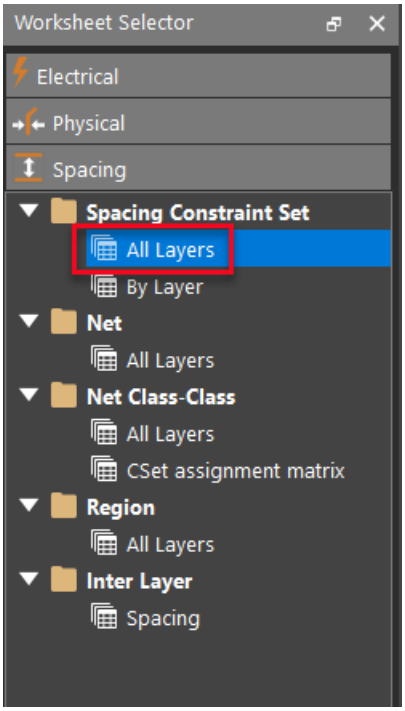
1. Continue working in the same board. Alternately, you can follow the steps below to begin with a board that has the Physical constraints set up.

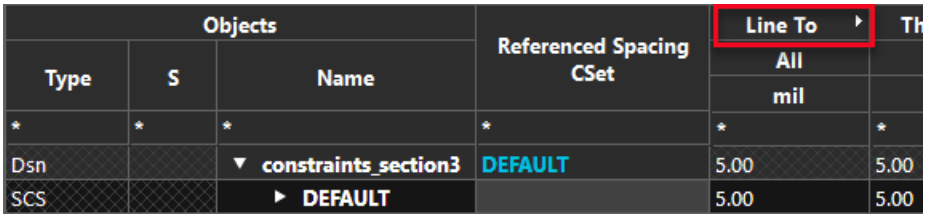
    a. Open **constraints.brd**.

    b. Select **Setup > Constraints > Constraint Manager** to open CM.

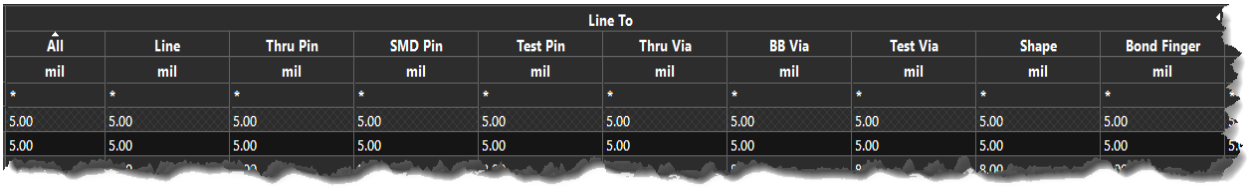
    c. In CM, select **File > Import > Constraints**.

    d. Select **phys_cns.dcfx** and click **Open**.





| Objects | | | Referenced Spacing CSet | Line To | Th |
|---|---|---|---|---|---|
| Type | S | Name | | All | |
| | | | | mil | |
| * | * | * | * | * | * |
| Dsn | | constraints_section3 | DEFAULT | 5.00 | 5.00 |
| SCS | | DEFAULT | | 5.00 | 5.00 |



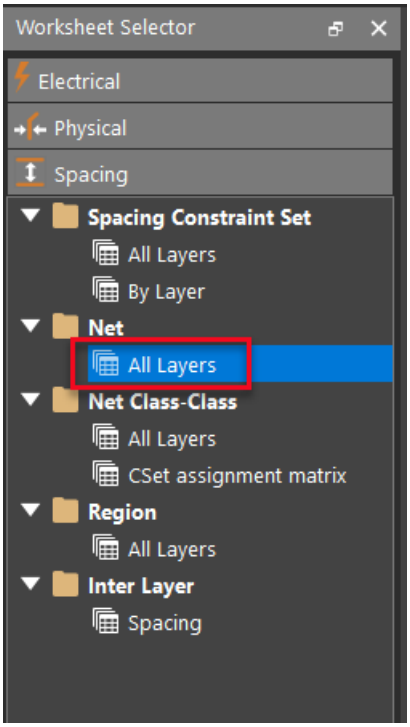
| Line To | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| All | Line | Thru Pin | SMD Pin | Test Pin | Thru Via | BB Via | Test Via | Shape | Bond Finger |
| mil | mil | mil | mil | mil | mil | mil | mil | mil | mil |
| * | * | * | * | * | * | * | * | * | * |
| 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 |
| 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 |

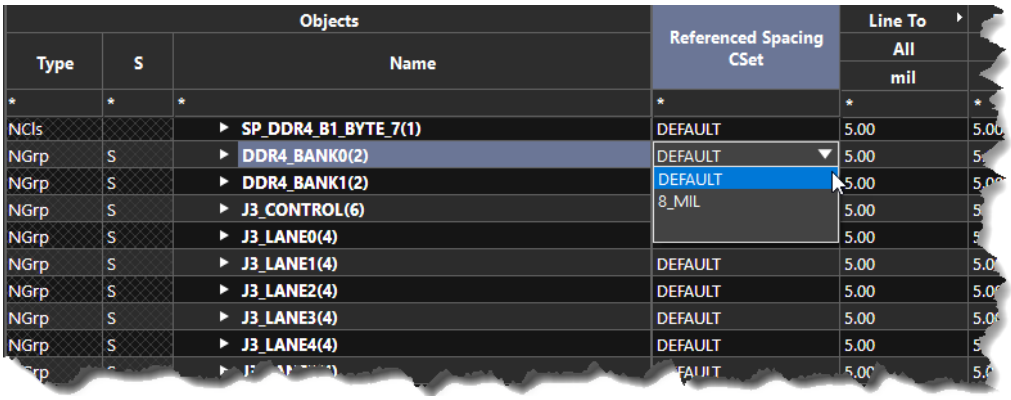
4. Right-click on the **DEFAULT** SCSet and select **Create > Spacing CSet**.
5. In the Create Spacing CSet form, enter **8_mil** and click **Ok**.

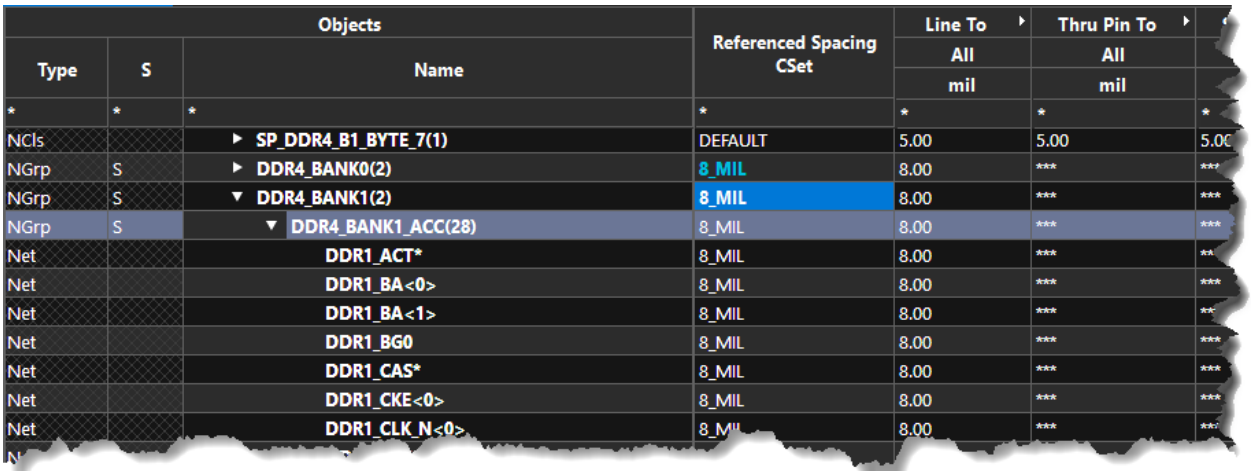
| Objects | | | Referenced Spacing CSet | Line To | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Type | S | Name | | All | Line | Thru Pin | SMD Pin | Test Pin | |
| | | | | mil | mil | mil | mil | mil | |
| * | * | * | * | * | * | * | * | * | * |
| Dsn | | constraints_section3 | DEFAULT | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 |
| SCS | | DEFAULT | | 5.00 | | 5.00 | 5.00 | 5.00 | 5.00 |
| SCS | | 8_MIL | | 8.00 | 8.00 | 8.00 | 8.00 | 8.00 | 8.00 |

## Lab 7: Assigning the Spacing Constraint Set

SCSet will be assigned to the DDR4_BANK0 and DDR4_BANK1 net groups.





| Objects | | | Referenced Spacing CSet | Line To | Thru Pin To | |
|---|---|---|---|---|---|---|
| Type | S | Name | | All | All | |
| | | | | mil | mil | |
| * | * | * | * | * | * | * |
| NCls | | ▶ SP_DDR4_B1_BYTE_7(1) | DEFAULT | 5.00 | 5.00 | 5.0 |
| NGrp | S | ▶ DDR4_BANK0(2) | 8_MIL | 8.00 | *** | *** |
| NGrp | S | ▼ DDR4_BANK1(2) | 8_MIL | 8.00 | *** | *** |
| NGrp | S | ▼ DDR4_BANK1_ACC(28) | 8_MIL | 8.00 | *** | *** |
| Net | | DDR1_ACT* | 8_MIL | 8.00 | *** | *** |
| Net | | DDR1_BA<0> | 8_MIL | 8.00 | *** | *** |
| Net | | DDR1_BA<1> | 8_MIL | 8.00 | *** | *** |
| Net | | DDR1_BG0 | 8_MIL | 8.00 | *** | *** |
| Net | | DDR1_CAS* | 8_MIL | 8.00 | *** | *** |
| Net | | DDR1_CKE<0> | 8_MIL | 8.00 | *** | *** |
| Net | | DDR1_CLK_N<0> | 8_MIL | 8.00 | *** | *** |

# Module 3: Constraint Regions

Constraint regions can be used to create special routing areas in the design. These regions can have different spacing rules, different physical rules, or both.

A **Region** (Rgn) is a bounded area of the design within which the different width and clearance constraints apply to all nets that cross the boundary. A region is defined by drawing a geometric shape, or a group of shapes, on a subclass layer in Allegro PCB Editor.

A **Region Class** (RCls) lets you constrain the nets of a Net Class within a region differently than the original constraints on that region. The constraints on the nets of a Region Class are exceptions to the constraints originally applied to the region. A region is more generic; a Region Class allows more specific exceptions to be defined.

A **Region Class-Class** (RCC) lets you specify the minimum spacing between nets of different Net Classes within a region.

Regions apply to the Physical, Spacing, and Same Net Spacing domains. Constrain a region by either referencing a CSet or setting overrides directly on the Region object.

## Lab 8: Creating a Region

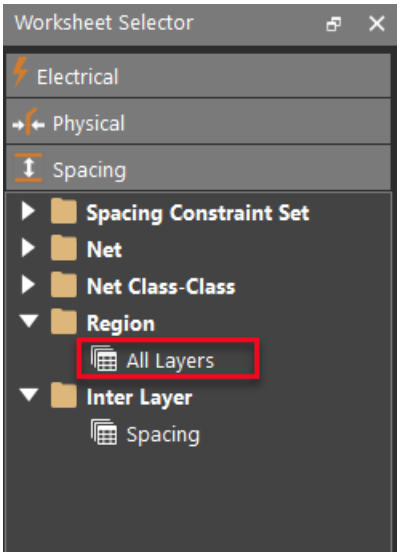
1. Continue working in the same board. Alternately, you can follow the steps below to begin with a board that has the Physical and Spacing constraints set up.

    a. Open **constraints.brd**.

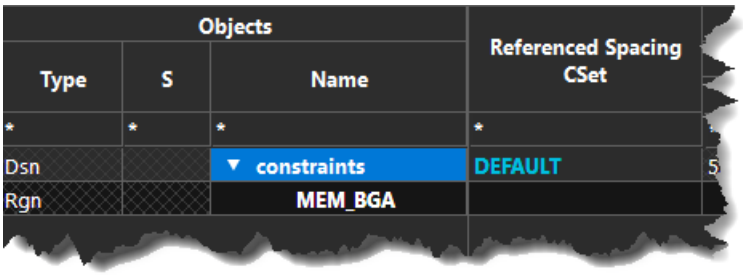
    b. Select **Setup > Constraints > Constraint Manager** to open CM.

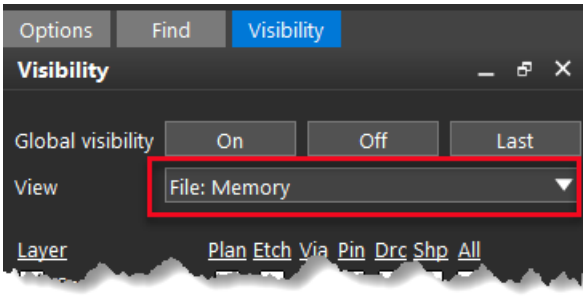
    c. In CM, select **File > Import > Constraints**.

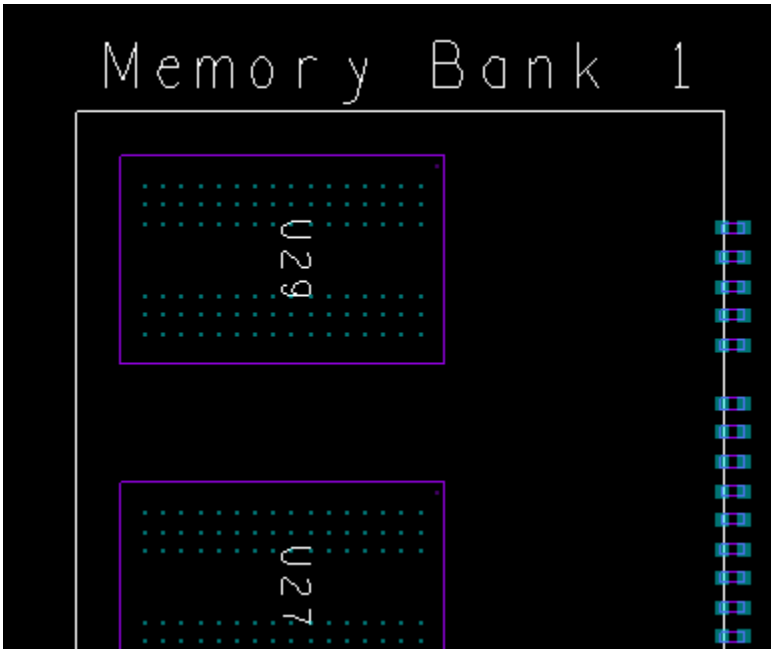
    d. Select **phys_spc_cns.dcfx**, and then click **Open**.




3. Select **Objects > Create > Region**.

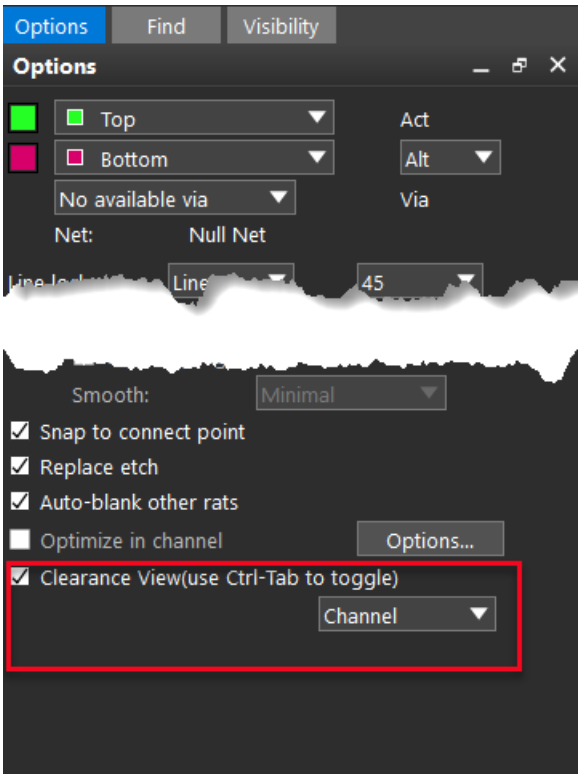


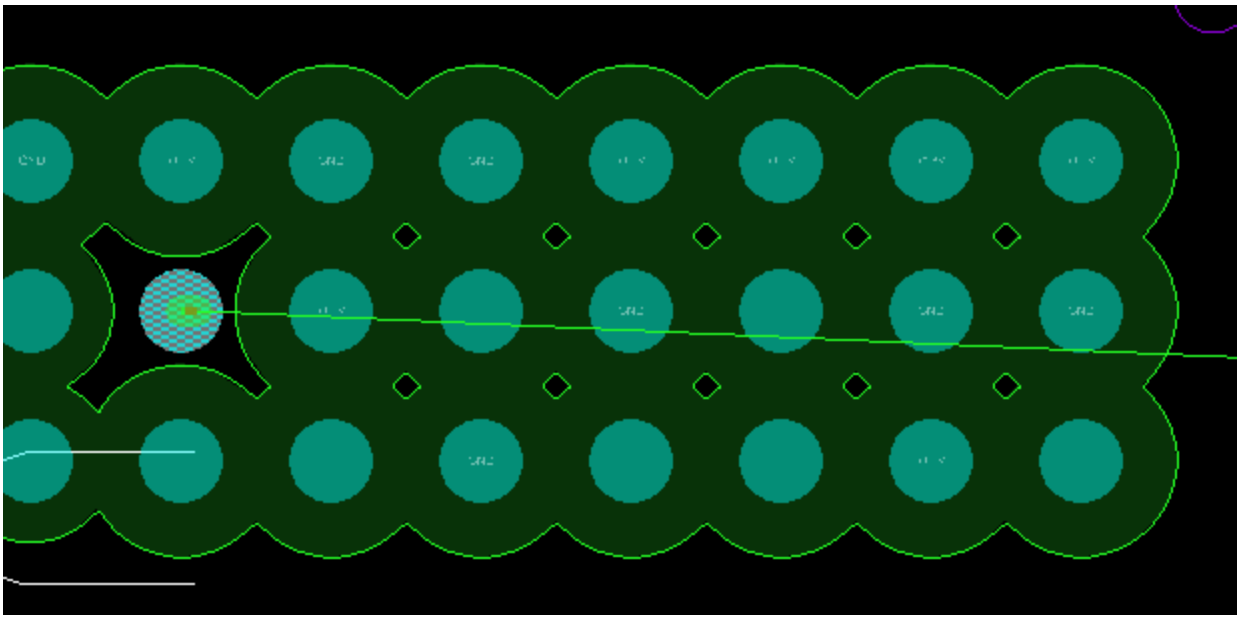



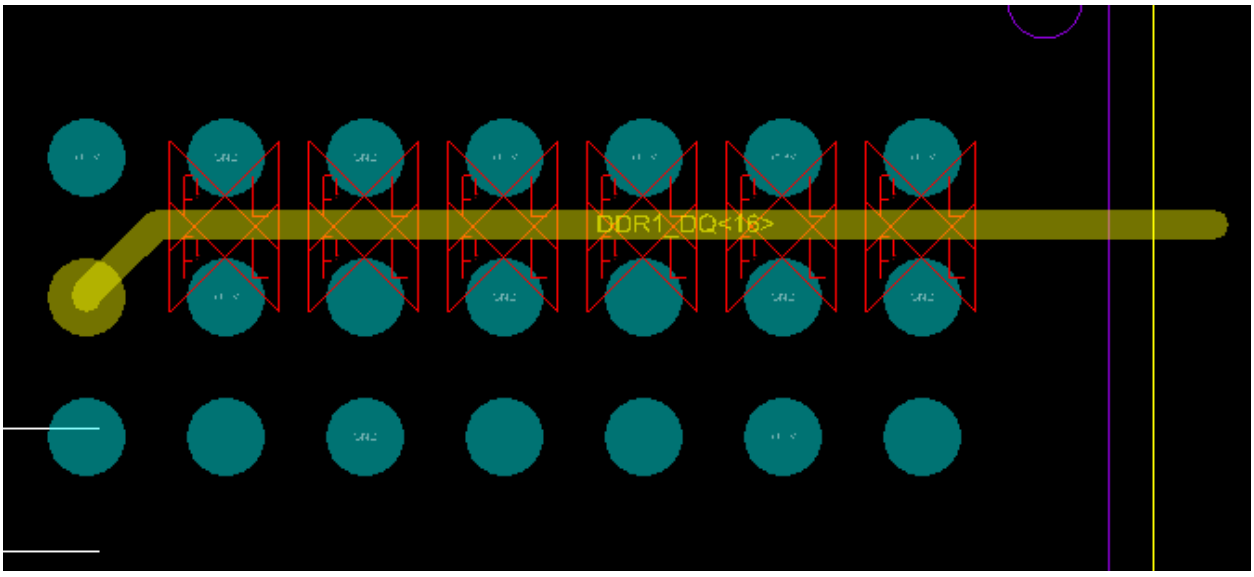



DRCs will be created when routing using the physical and spacing constraints, which are set on the nets going to these components. A region can be used to specify different constraints for the traces routed to the components.

7. Select **Route > Connect**.



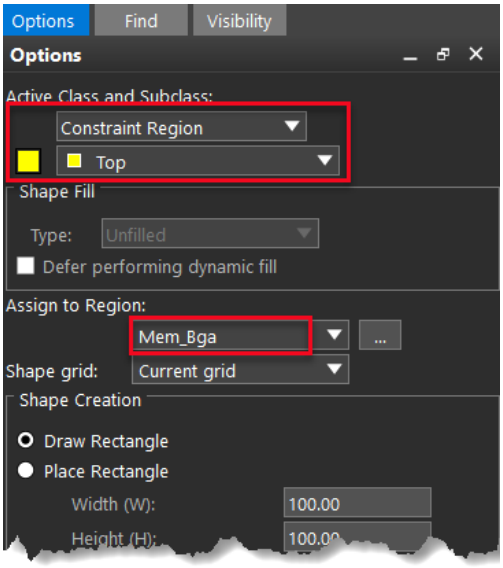


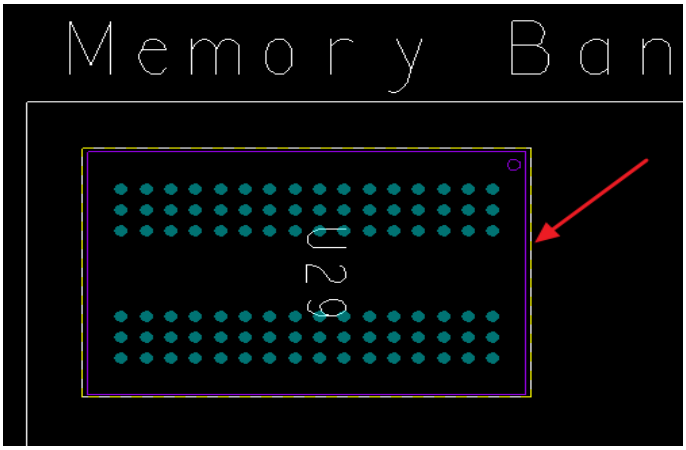



11. Right-click and select **Cancel** to exit the command without placing the trace.

12. A shape must be drawn to define the region on the Allegro canvas. Select **Shape > Rectangular**.

13. In the **Options** pane, set the **Active Class and Subclass** to **Constraint Region/Top**.

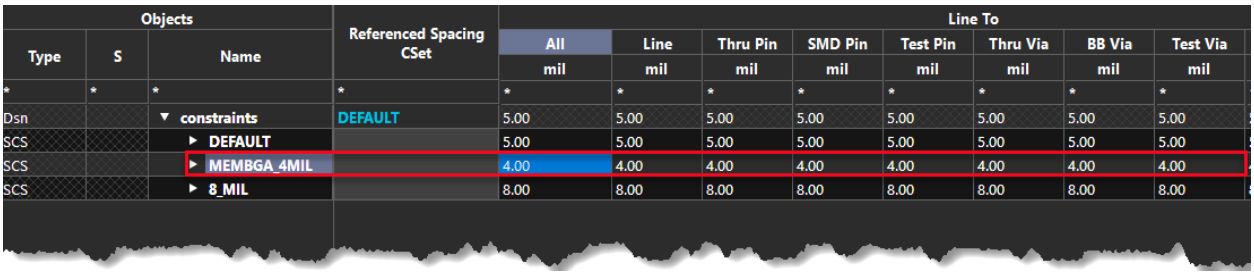



16. Right-click on the canvas and select **Done**.

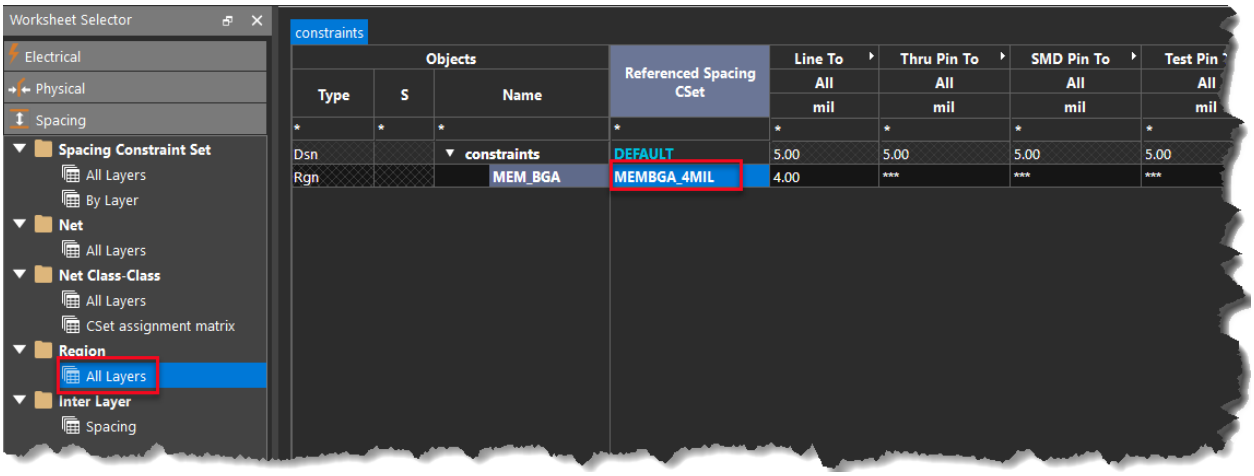
## Lab 9: Assigning Physical and Spacing Constraints to Region

1. In the Spacing domain in CM, select the **Spacing Constraint Set > All Layers** worksheet.
2. Right-click on the **8_MIL** SCSet and select **Create > Spacing CSet**.
3. In the **Create Spacing CSet** form, enter **membga_4mil** and click **Ok**.



| Objects | | | Referenced Spacing CSet | Line To | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Type | S | Name | | All | Line | Thru Pin | SMD Pin | Test Pin | Thru Via | BB Via | Test Via |
| | | | | mil | mil | mil | mil | mil | mil | mil | mil |
| * | * | * | * | * | * | * | * | * | * | * | * |
| Dsn | | constraints | DEFAULT | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 |
| SCS | | DEFAULT | | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 |
| SCS | | MEMBGA_4MIL | | 4.00 | 4.00 | 4.00 | 4.00 | 4.00 | 4.00 | 4.00 | 4.00 |
| SCS | | 8_MIL | | 8.00 | 8.00 | 8.00 | 8.00 | 8.00 | 8.00 | 8.00 | 8.00 |

5. Select the **Region > All Layers** worksheet.

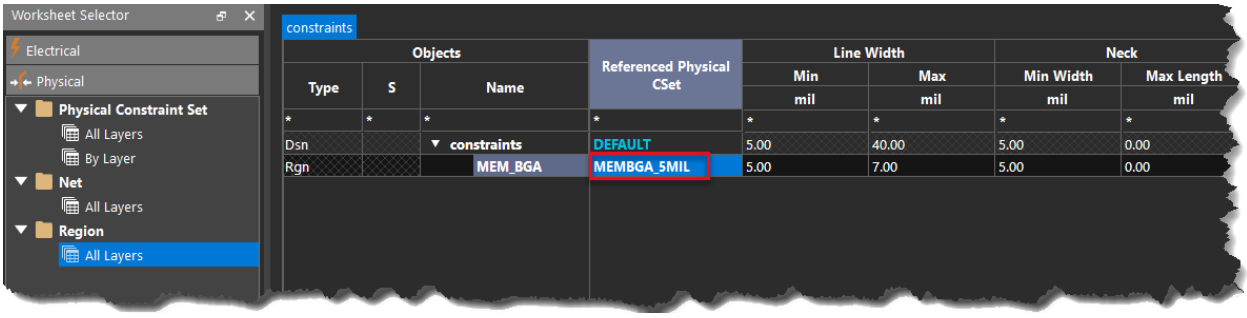



7. In the Physical domain, select the **Physical Constraint Set > All Layers** worksheet.
8. Right-click on the **DDR4_SE** PCSet and select **Create > Physical CSet**.
9. In the **Create Physical CSet** form, enter **membga_5mil** and click **Ok**.
10. Set the following constraints for the MEMBGA_5MIL PCSet:

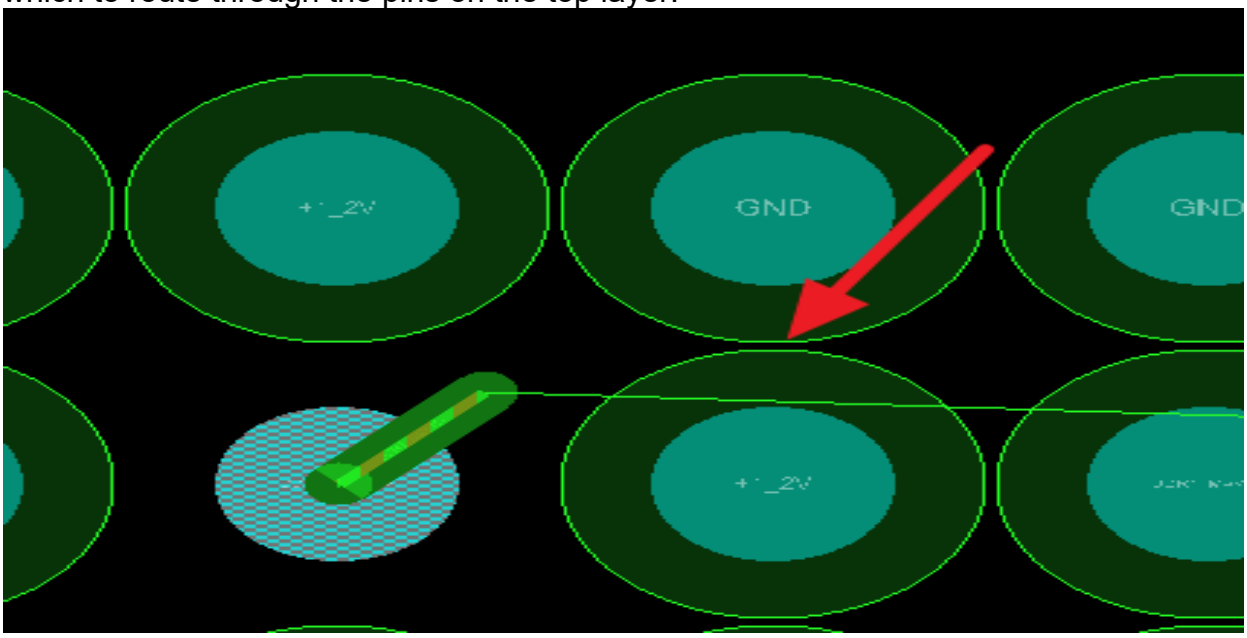
| | |
|---|---|
| **Min Line Width** | 5 |
| **Max Line Width** | 7 |
| **Min Neck Width** | 5 |
| **Max Neck Length** | 0 |
| **DP Min Line Spacing** | 4 |
| **DP Primary Gap** | 5 |
| **DP Neck Gap** | 0 |
| **DP (+) Tolerance** | 0.1 |
| **DP (-) Tolerance** | 0.1 |

11. Select the **Region > All Layers** worksheet.

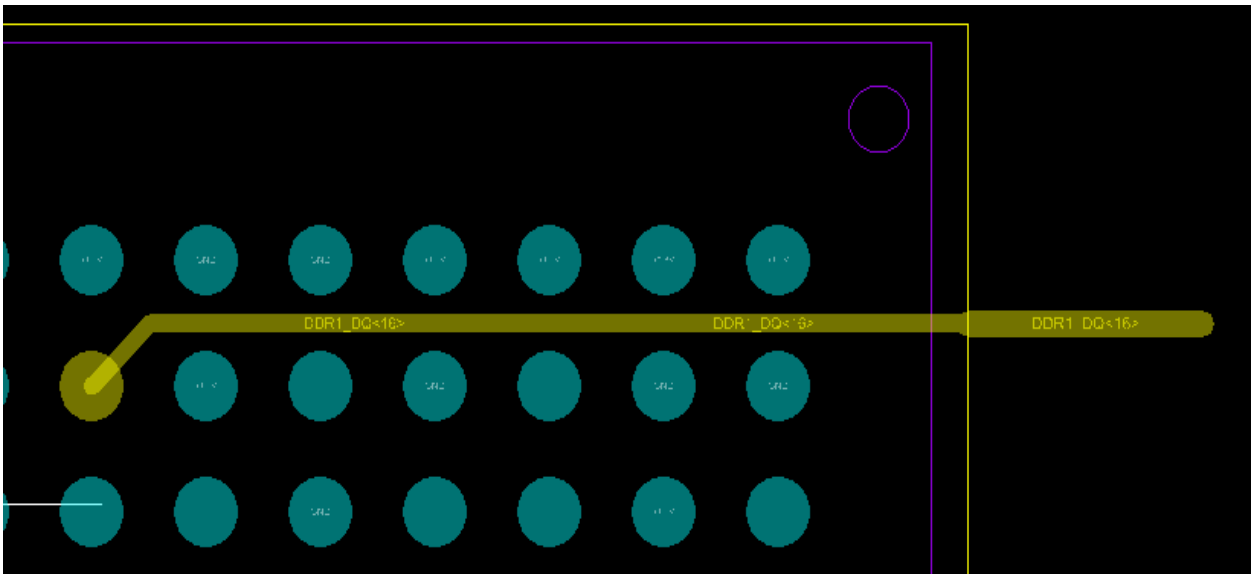
12. Assign the **MEMBGA_5MIL** PCSet to the **MEM_BGA** region.




13. In Allegro, use **Route > Connect** to begin a trace on the DDR1_DQ<16> net. With the **Clearance View** set to **Channel**, there is now a channel available in which to route through the pins on the top layer.



14. Continue routing outside of the region. You will see the trace width change as you cross the region border.




15. Right-click and select **Done**.

16. Select **File > Exit** to exit Allegro. You do not need to save the drawing. This completes this RAK.

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