cadence

Allegro Front-to-Back Flow – Backdrill, Post-Processing, and Report Generation

Rapid Adoption Kit (RAK)

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Purpose

The purpose of this RAK is to provide an overview of Allegro PCB Editor post-processing utilities used to complete a design prior to fabrication. This includes steps to generate backdrill data, thieving, artwork, NC drill legends, testpoints, and reports.

Audience

This document is intended for PCB designers, hardware designers, and engineers who use Allegro solutions.

Download

RAK testcase database, Scripts, and References can be found at ‘Attachments’ and ‘Related Solutions’ sections below the PDF.

This RAK pdf can be searched with the document ‘title’ on https://support.cadence.com.

Module 1: Backdrill

Today's high-speed digital signals present new challenges for hardware engineers. Passing high-frequency signals through plated through-holes in high layer count printed circuit boards and thick backplanes can significantly distort high-speed digital signals that pass through them. The unused portions of through-holes and vias that extend past their last connected layer are known as stubs. These stubs are the source of impedance discontinuities and signal reflections, which become more critical as data rates increase.

An effective method to manage these stubs is a board fabrication technique called backdrilling. This controlled depth drilling technique uses conventional numerically controlled drill equipment to remove the stubs. It can be performed from either side of the PCB and to multiple depths.

In this module, the **Backdrill Setup and Analysis** form will be used to identify problematic stubs on plated through-holes and vias on high-speed critical signals. This lab will provide an overview of the setup process prior to running backdrill on a design. The design has the `BACKDRILL_MAX_PTH_STUB` property attached to nets to identify backdrill candidates and minimum electrical stub requirements.

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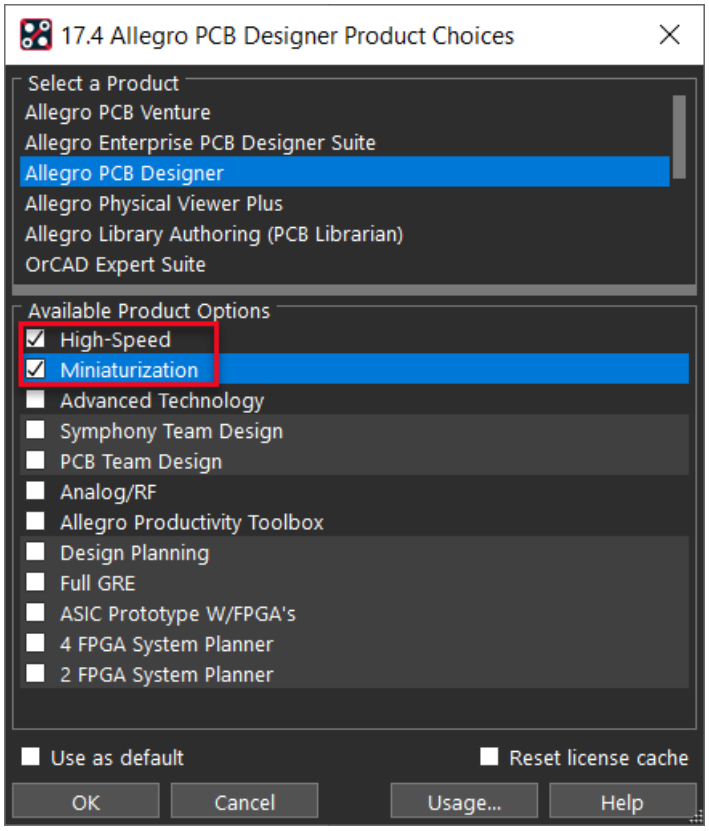
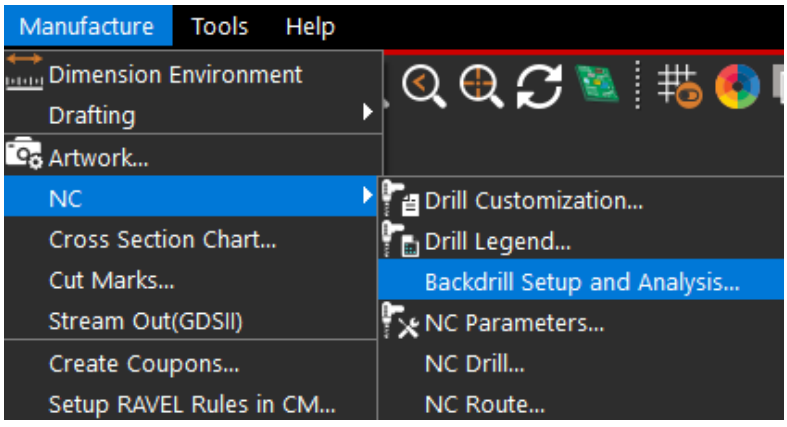
Lab 1: Backdrill Setup and Analysis

1. Open **start.brd** in Allegro PCB Designer. Select the **Allegro PCB Designer** license with the **High-Speed** and **Miniaturization** options in the **Product Choices** window.



2. In Allegro, select **Manufacture > NC > Backdrill Setup and Analysis**.



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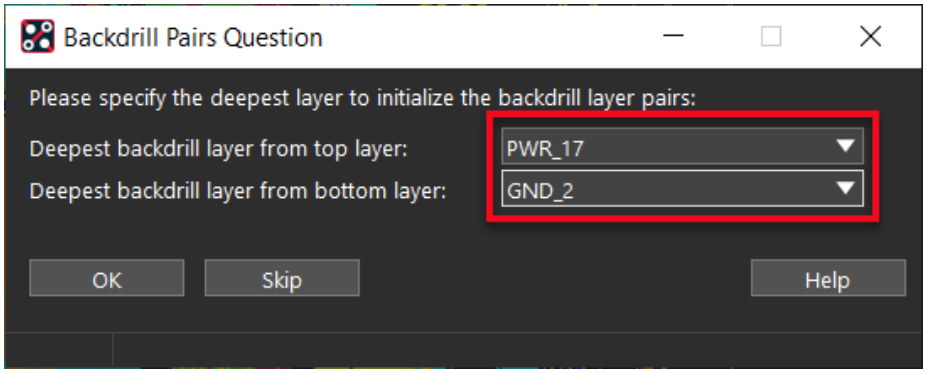
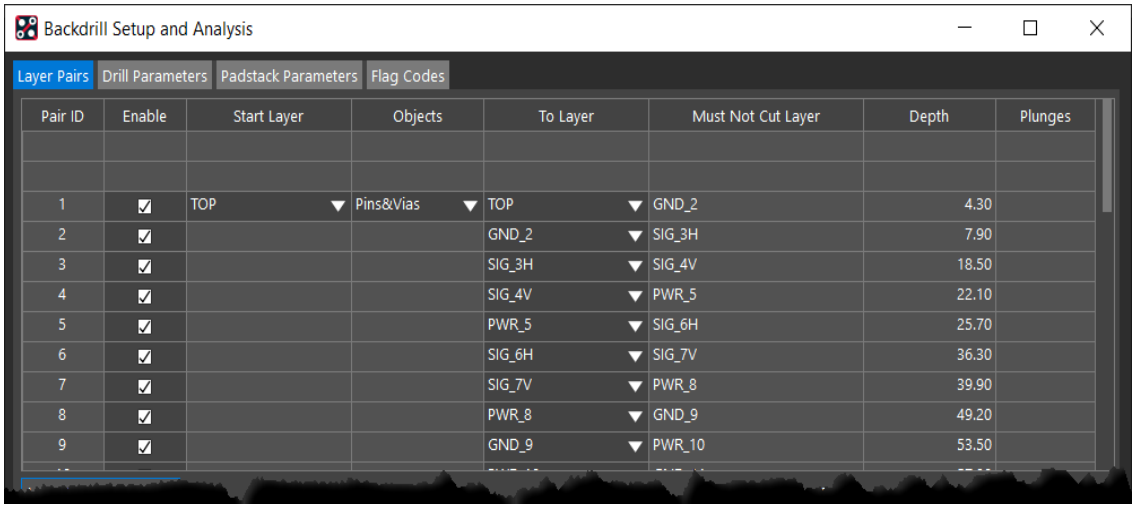
3. The **Backdrill Pairs Question** form can be used to create backdrill layer pairs by selecting the deepest backdrill layer for each side of the board. Select **PWR_17** for **Deepest backdrill layer from top layer** and **GND_2** for **Deepest backdrill layer from bottom layer**, then select **OK**.



The **Backdrill Setup and Analysis** form displays each layer pair that was generated.



Pair ID	Enable	Start Layer	Objects	To Layer	Must Not Cut Layer	Depth	Plunges
1	☑	TOP	Pins&Vias	TOP	GND_2	4.30	
2	☑			GND_2	SIG_3H	7.90	
3	☑			SIG_3H	SIG_4V	18.50	
4	☑			SIG_4V	PWR_5	22.10	
5	☑			PWR_5	SIG_6H	25.70	
6	☑			SIG_6H	SIG_7V	36.30	
7	☑			SIG_7V	PWR_8	39.90	
8	☑			PWR_8	GND_9	49.20	
9	☑			GND_9	PWR_10	53.50	

The layer pairs contain:

- **Start Layer** – start layer of backdrill
- **Objects** – objects to be backdrilled (pins, vias, or pins and vias)
- **To Layer** – last layer to be backdrilled
- **Must Not Cut Layer** – layer with connection that requires conductivity
- **Depth** – depth from the Start layer to the outside surface of the Must Not Cut layer
- **Plunges** – number of possible backdrill locations

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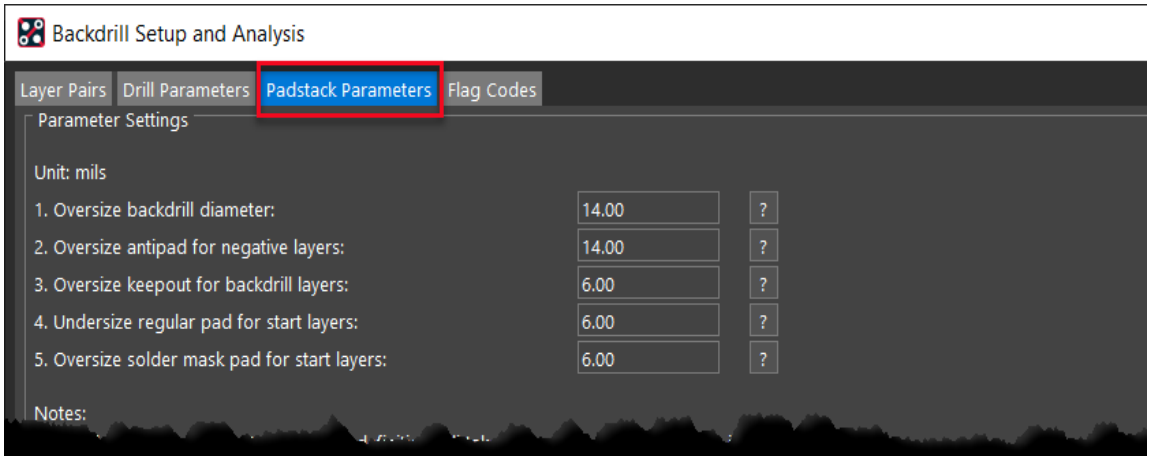
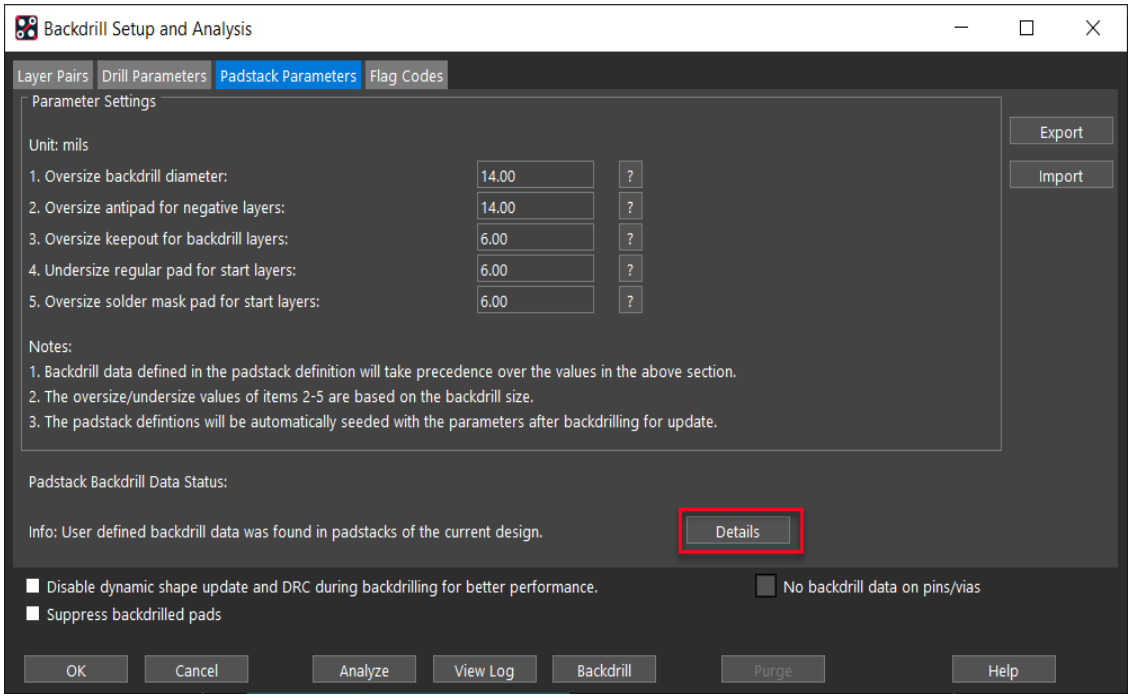
4. Select the **Padstack Parameters** tab. The padstack parameter values are used to update design-level padstacks that do not have any backdrill data defined in the library or manually entered in the design.



5. Select the **Details** button.



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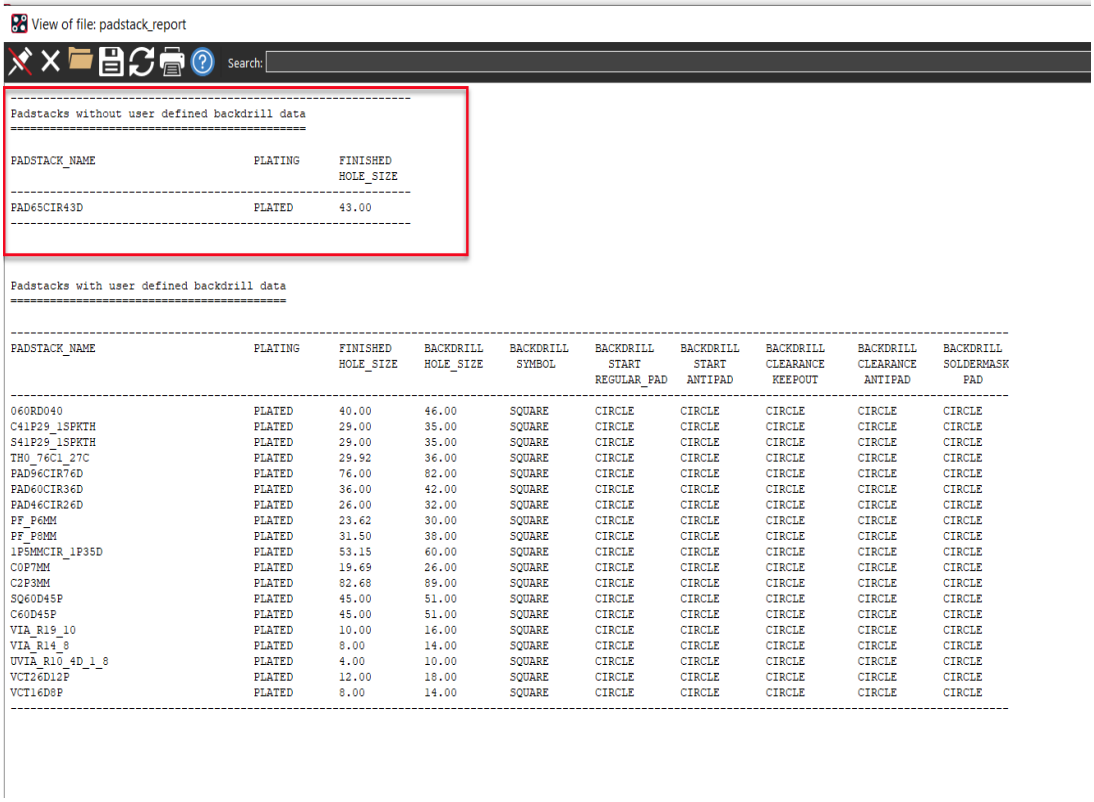
This will display the *padstack_report.log* file. This report lists padstacks with and without user-defined backdrill data. Notice that **PAD65CIR43D** is the only padstack without user-defined backdrill data.



View of file: padstack_report

Search:

Padstacks without user defined backdrill data

PADSTACK_NAME	PLATING	FINISHED HOLE_SIZE
PAD65CIR43D	PLATED	43.00

Padstacks with user defined backdrill data

PADSTACK_NAME	PLATING	FINISHED HOLE_SIZE	BACKDRILL HOLE_SIZE	BACKDRILL SYMBOL	BACKDRILL START REGULAR_PAD	BACKDRILL START ANTIPAD	BACKDRILL CLEARANCE KEEPOUT	BACKDRILL CLEARANCE ANTIPAD	BACKDRILL SOLDERMASK PAD
060RD040	PLATED	40.00	46.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
C41P29_1SPKTH	PLATED	29.00	35.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
S41P29_1SPKTH	PLATED	29.00	35.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
TH0_76C1_27C	PLATED	29.92	36.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
PAD96CIR76D	PLATED	76.00	82.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
PAD60CIR36D	PLATED	36.00	42.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
PAD46CIR26D	PLATED	26.00	32.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
PF_P6MM	PLATED	23.62	30.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
PF_P8MM	PLATED	31.50	38.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
1P5MMCIR_1P35D	PLATED	53.15	60.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
C0P7MM	PLATED	19.69	26.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
C2P3MM	PLATED	82.68	89.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
SQ60D45P	PLATED	45.00	51.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
C60D45P	PLATED	45.00	51.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
VIA_R19_10	PLATED	10.00	16.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
VIA_R14_8	PLATED	8.00	14.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
UVIA_R10_4D_1_8	PLATED	4.00	10.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
VCT26D12P	PLATED	12.00	18.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE
VCT16D8P	PLATED	8.00	14.00	SQUARE	CIRCLE	CIRCLE	CIRCLE	CIRCLE	CIRCLE

6. Close the report.

7. Minimize or move the **Backdrill Setup and Analysis** form to the side.

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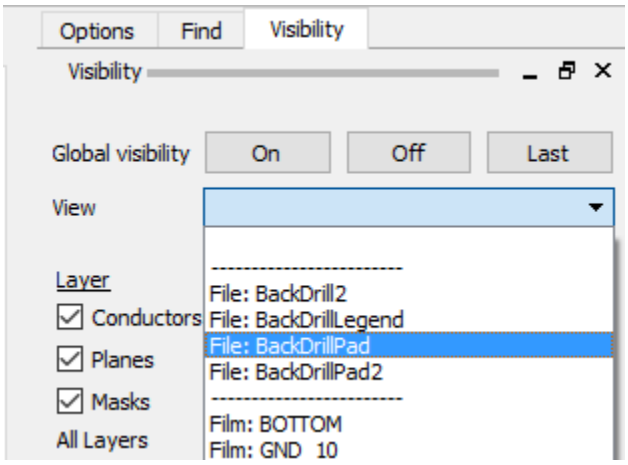
Lab 2: Padstack Editor Backdrill Data Support

The Pad Editor will be used to enter backdrill information into the **PAD65CIR43D** padstack. This padstack will then be updated to the design.

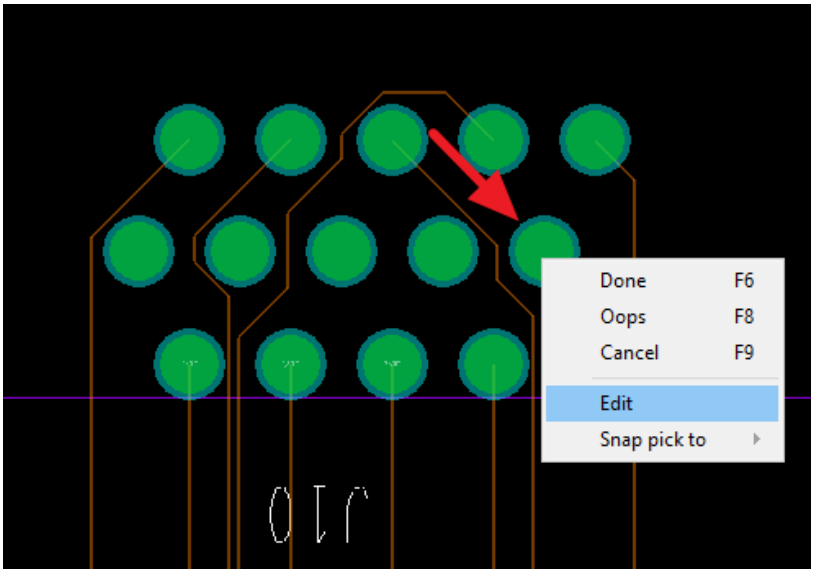
1. In the **Visibility** tab in Allegro, select the **BackDrillPad** view from the **View** pulldown.



   This will zoom into an area that contains the **PAD65CIR43D** padstack.

2. Select **Tools > Padstack > Modify Design Padstack**.

3. Click on the pad indicated by the red arrow and right-click and select **Edit**.



4. In the Pad Editor, select the **Secondary Drill** tab and enable **Backdrill**.

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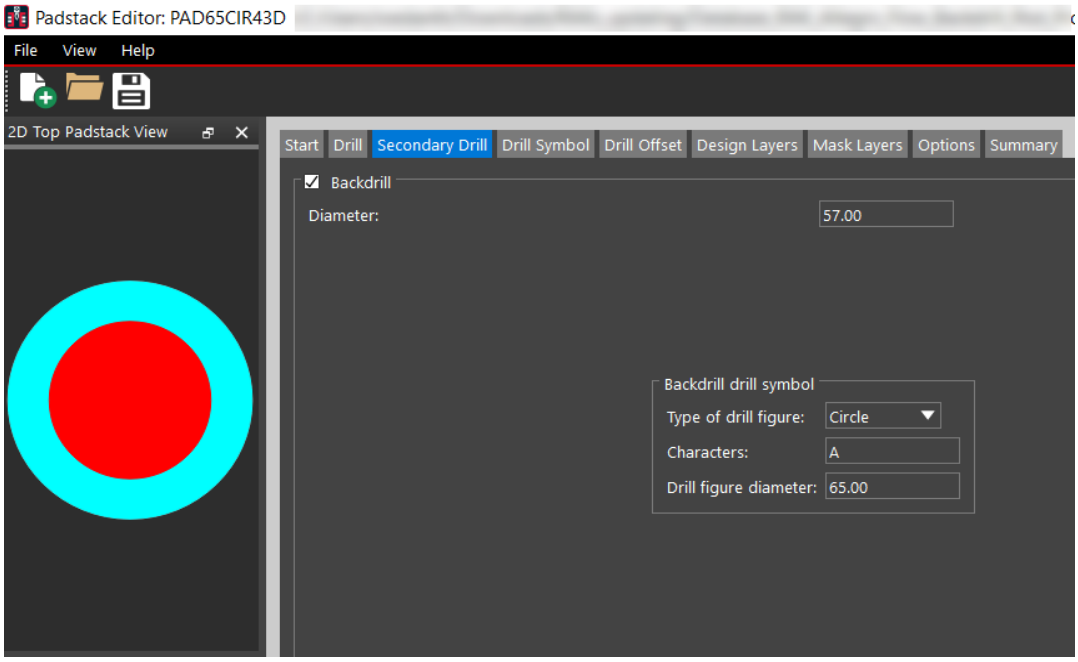
5. Set the following:

   - Diameter: 57
   - Type of drill figure: Circle
   - Characters: A
   - Drill figure diameter: 65



6. Select the **Design Layers** tab.

7. Fill out the following values for the **BACKDRILL START** layer:

   - Regular Pad
     Geometry: Circle
     Diameter: 51

   - Anti Pad
     Geometry: Circle
     Diameter: 71

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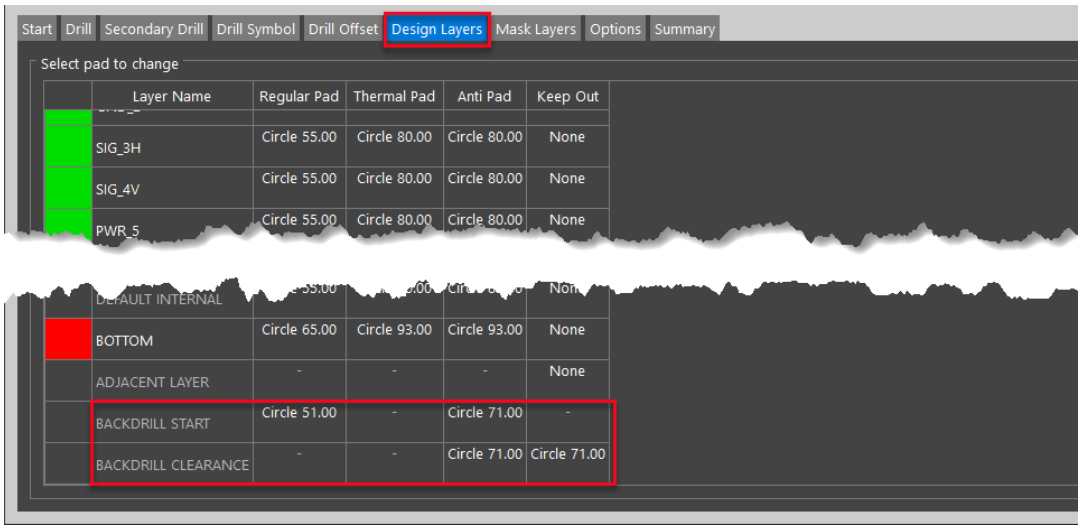
8. Fill out the following values for the **BACKDRILL CLEARANCE** layer:

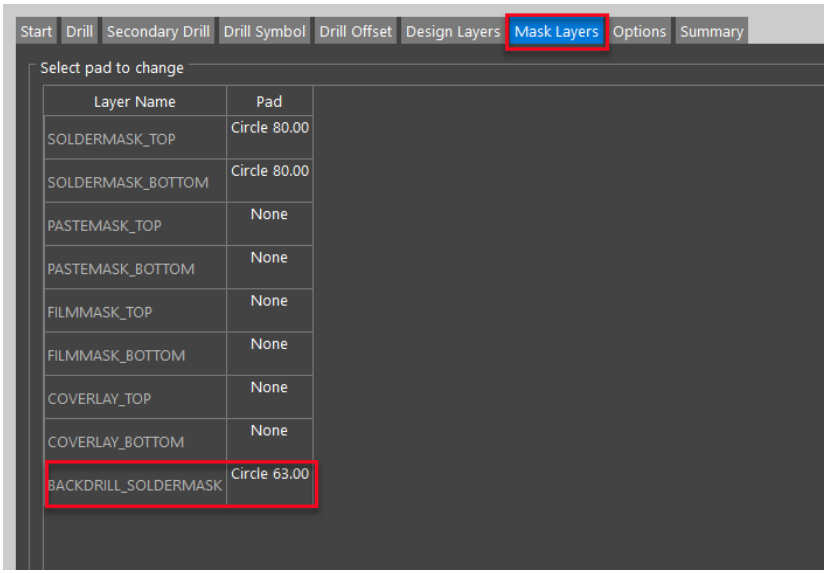
   - Anti Pad
     Geometry: Circle
     Diameter: 71

   - Keep Out
     Geometry: Circle
     Diameter: 71



9. Select the **Mask Layers** tab.

10. Set the **BACKDRILL_SOLDERMASK** pad to be a **Circle** with a **Diameter** of **63**.



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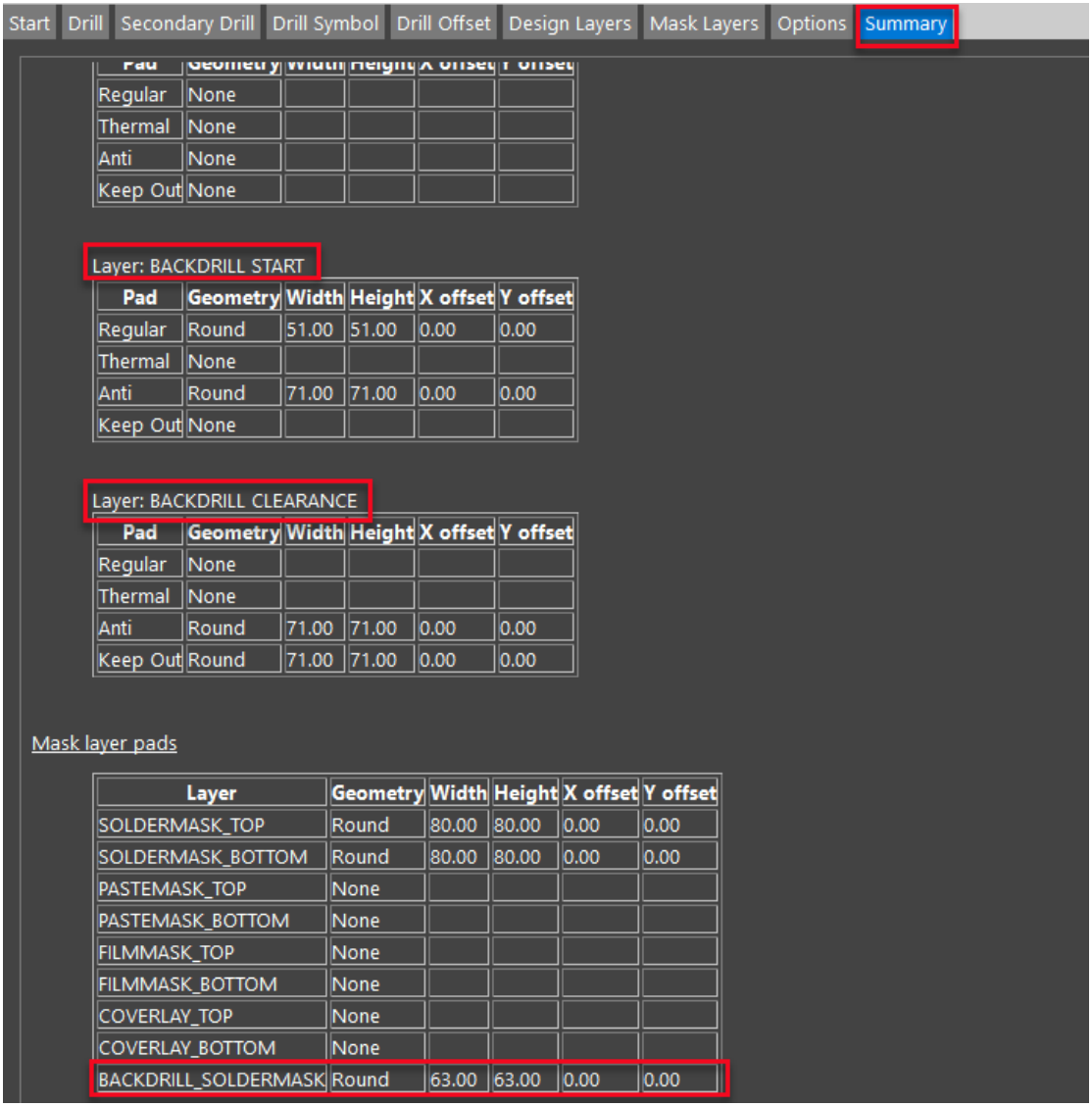
11. Select the **Summary** tab. Scroll to the bottom and review the backdrill sizes that were entered.



Pad	Geometry	Width	Height	X offset	Y offset
Regular	None				
Thermal	None				
Anti	None				
Keep Out	None				

Layer: BACKDRILL START

Pad	Geometry	Width	Height	X offset	Y offset
Regular	Round	51.00	51.00	0.00	0.00
Thermal	None				
Anti	Round	71.00	71.00	0.00	0.00
Keep Out	None				

Layer: BACKDRILL CLEARANCE

Pad	Geometry	Width	Height	X offset	Y offset
Regular	None				
Thermal	None				
Anti	Round	71.00	71.00	0.00	0.00
Keep Out	Round	71.00	71.00	0.00	0.00

Mask layer pads

Layer	Geometry	Width	Height	X offset	Y offset
SOLDERMASK_TOP	Round	80.00	80.00	0.00	0.00
SOLDERMASK_BOTTOM	Round	80.00	80.00	0.00	0.00
PASTEMASK_TOP	None				
PASTEMASK_BOTTOM	None				
FILMMASK_TOP	None				
FILMMASK_BOTTOM	None				
COVERLAY_TOP	None				
COVERLAY_BOTTOM	None				
BACKDRILL_SOLDERMASK	Round	63.00	63.00	0.00	0.00

12. Select **File > Update to Design and Exit**.

13. Restore the **Backdrill Setup and Analysis** form. Select the **Layer Pairs** tab and click on the **Layer Pair Initialization** button.

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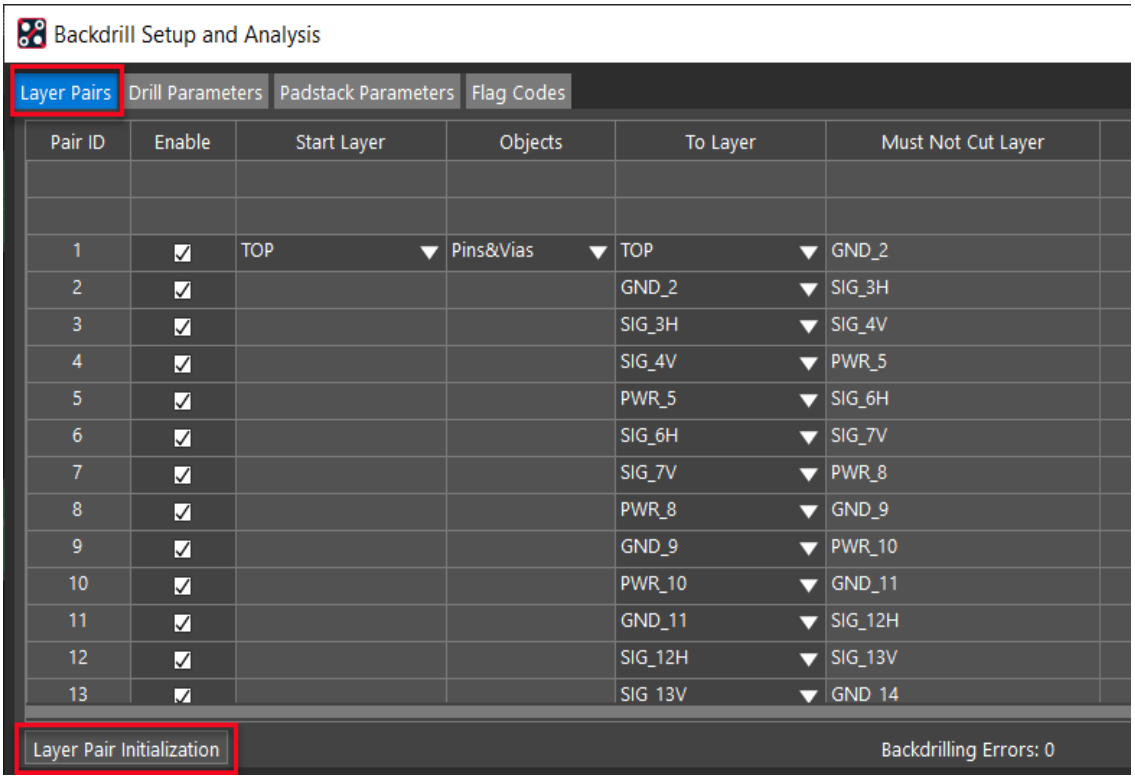
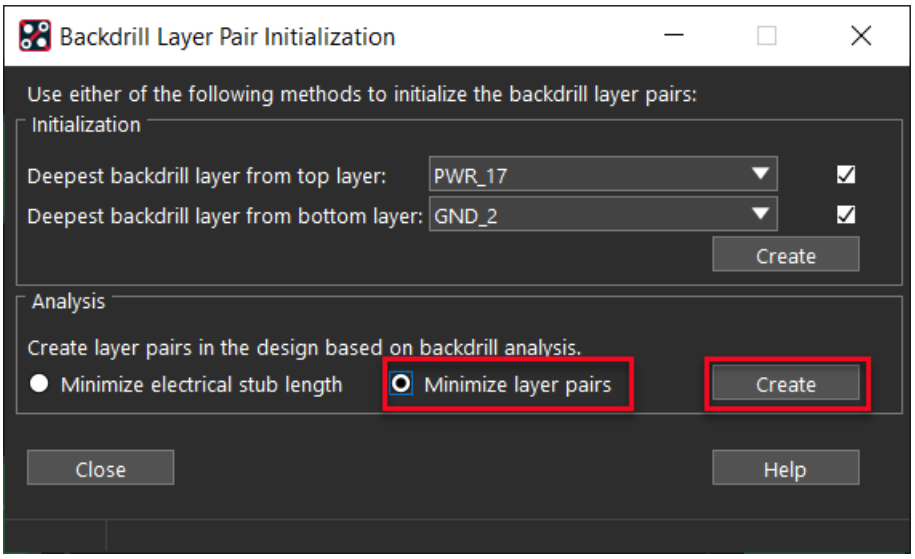


14. In the **Backdrill Layer Pair Initialization** form, select the **Minimize layer pairs** radio button, then select **Create** to create the backdrill layer pairs based on the backdrill analysis of the design.



15. Close the form.

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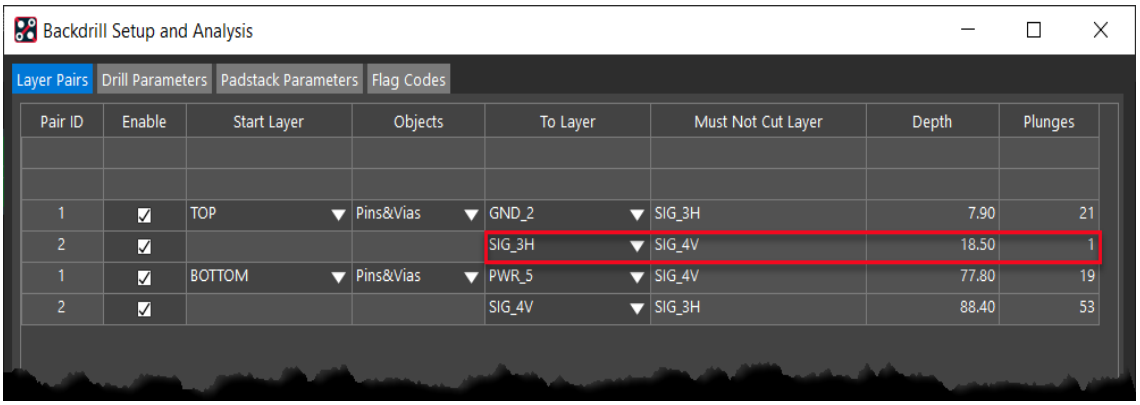
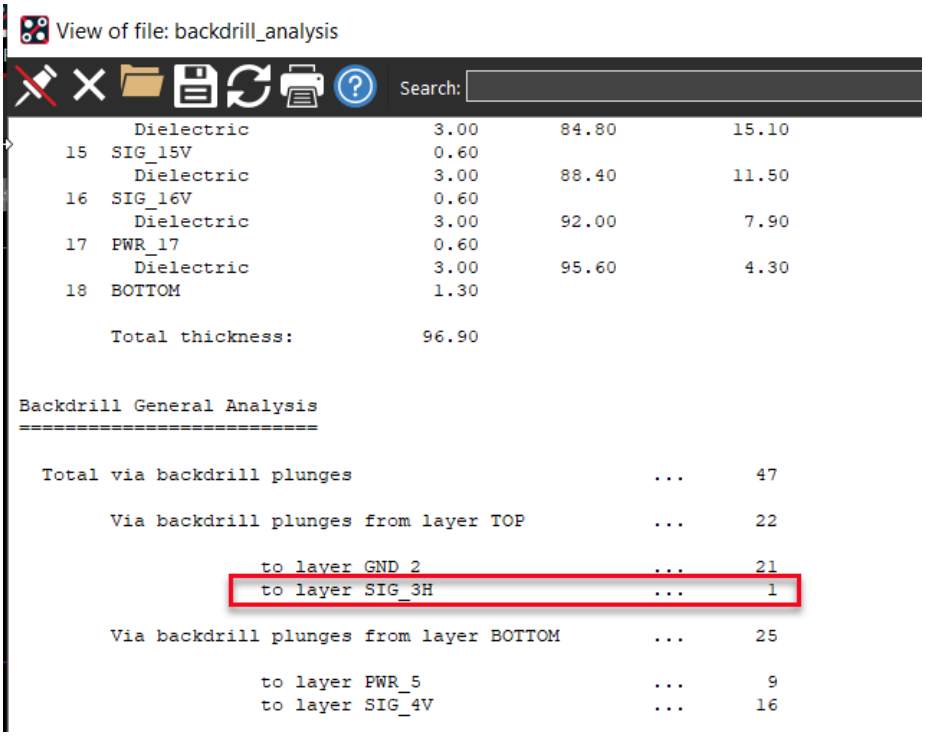
16. Notice in the **Backdrill Setup and Analysis** form that the row shown below only has **1** plunge. This means that the Must Not Cut Layer (**SIG_4V**) has only one location identified for backdrilling.



If this trace could be rerouted on **SIG_3H**, the TOP to SIG_3H backdrill layer pair could be eliminated, reducing the backdrill cost.

17. Click the **View Log** button.

18. In the backdrill_analysis report, scroll down to the **Total via backdrill plunges** section. The backdrill candidate is on a via going to the **SIG_3H** layer.



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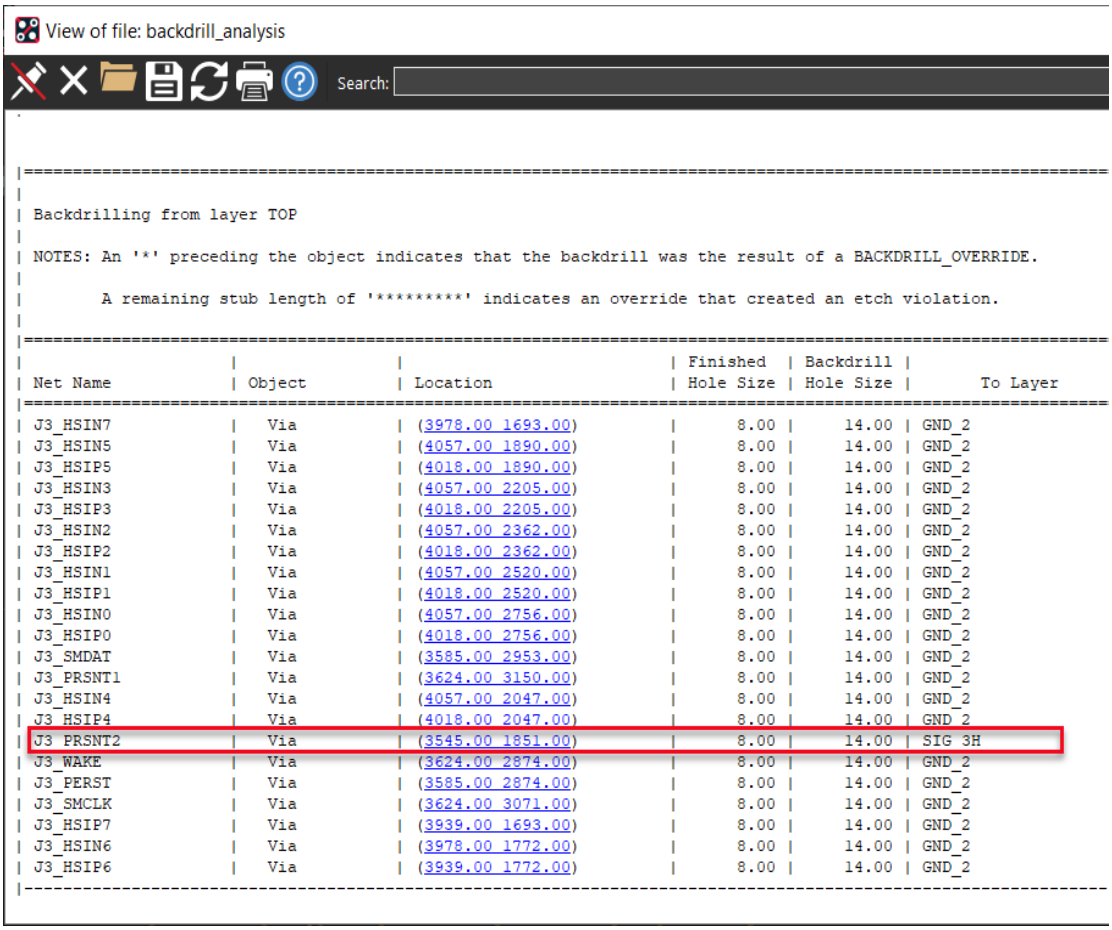
19. Scroll down further to the **Backdrilling from layer TOP** section. The via identified above is on the **J3_PRSNT2** net.



Backdrilling from layer TOP

NOTES: An '*' preceding the object indicates that the backdrill was the result of a BACKDRILL_OVERRIDE.

A remaining stub length of '**********' indicates an override that created an etch violation.

Net Name	Object	Location	Finished Hole Size	Backdrill Hole Size	To Layer
J3_HSIN7	Via	(3978.00 1693.00)	8.00	14.00	GND_2
J3_HSIN5	Via	(4057.00 1890.00)	8.00	14.00	GND_2
J3_HSIP5	Via	(4018.00 1890.00)	8.00	14.00	GND_2
J3_HSIN3	Via	(4057.00 2205.00)	8.00	14.00	GND_2
J3_HSIP3	Via	(4018.00 2205.00)	8.00	14.00	GND_2
J3_HSIN2	Via	(4057.00 2362.00)	8.00	14.00	GND_2
J3_HSIP2	Via	(4018.00 2362.00)	8.00	14.00	GND_2
J3_HSIN1	Via	(4057.00 2520.00)	8.00	14.00	GND_2
J3_HSIP1	Via	(4018.00 2520.00)	8.00	14.00	GND_2
J3_HSIN0	Via	(4057.00 2756.00)	8.00	14.00	GND_2
J3_HSIP0	Via	(4018.00 2756.00)	8.00	14.00	GND_2
J3_SMDAT	Via	(3585.00 2953.00)	8.00	14.00	GND_2
J3_PRSNT1	Via	(3624.00 3150.00)	8.00	14.00	GND_2
J3_HSIN4	Via	(4057.00 2047.00)	8.00	14.00	GND_2
J3_HSIP4	Via	(4018.00 2047.00)	8.00	14.00	GND_2
J3_PRSNT2	Via	(3545.00 1851.00)	8.00	14.00	SIG_3H
J3_WAKE	Via	(3624.00 2874.00)	8.00	14.00	GND_2
J3_PERST	Via	(3585.00 2874.00)	8.00	14.00	GND_2
J3_SMCLK	Via	(3624.00 3071.00)	8.00	14.00	GND_2
J3_HSIP7	Via	(3939.00 1693.00)	8.00	14.00	GND_2
J3_HSIN6	Via	(3978.00 1772.00)	8.00	14.00	GND_2
J3_HSIP6	Via	(3939.00 1772.00)	8.00	14.00	GND_2

20. Click on the link for the via coordinates to zoom into the via in the Allegro canvas. You may need to zoom in or select the **BackDrill2** view from the pulldown in the **Visibility** pane.

    The red box shown below indicates the location of the via. The trace indicated by the arrow is currently routed on the **Sig_4V** layer. If this trace can be moved to **SIG_3H**, the TOP to SIG_3H backdrill layer pair can be eliminated.

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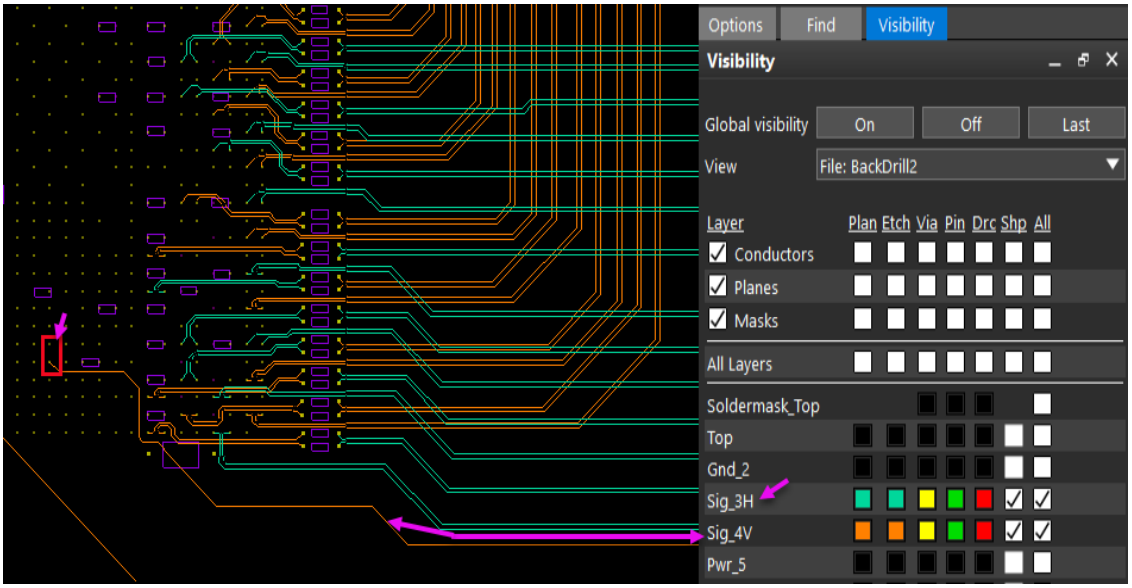
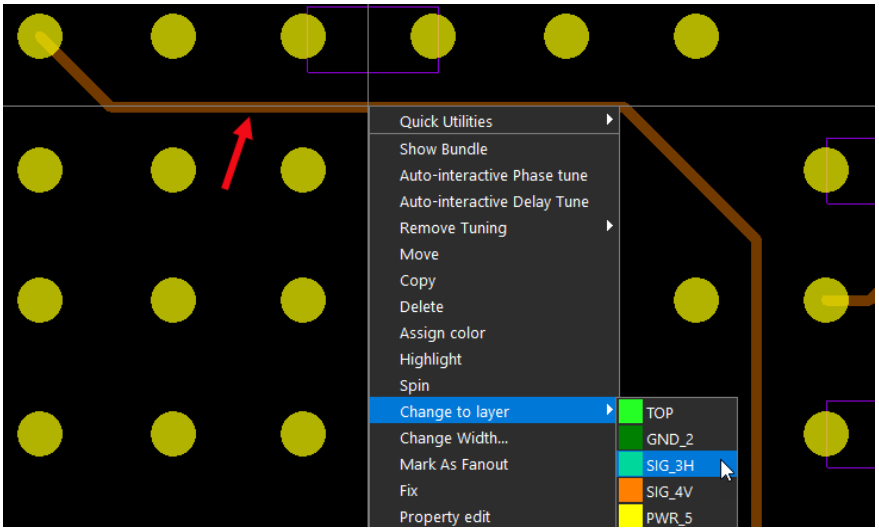


21. If you are not already in the Etch Edit application mode, select **Setup > Application Mode > Etch Edit**.

22. Right-click on the trace and select **Change to layer > SIG_3H**.



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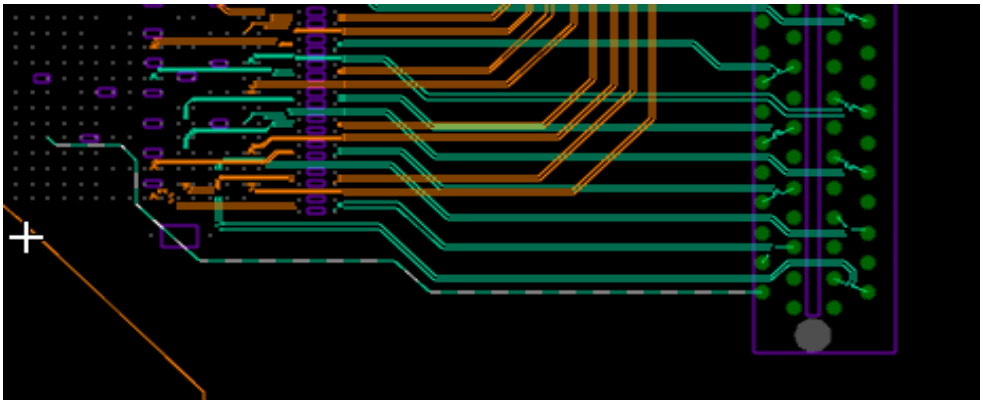
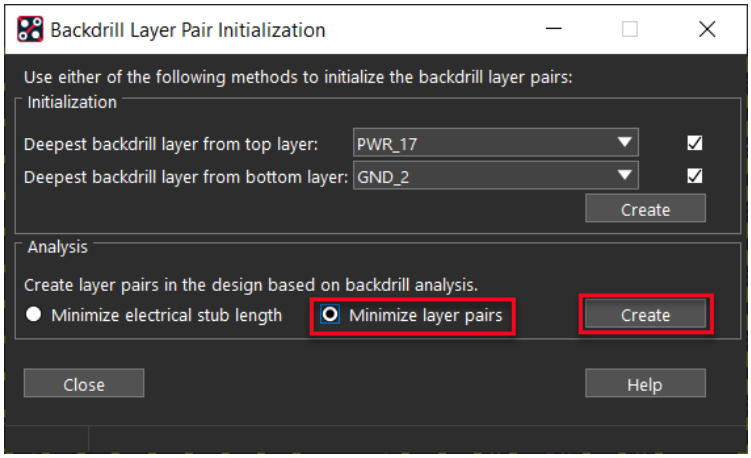
The trace is highlighted and displayed in the color for the **SIG_3H** layer.

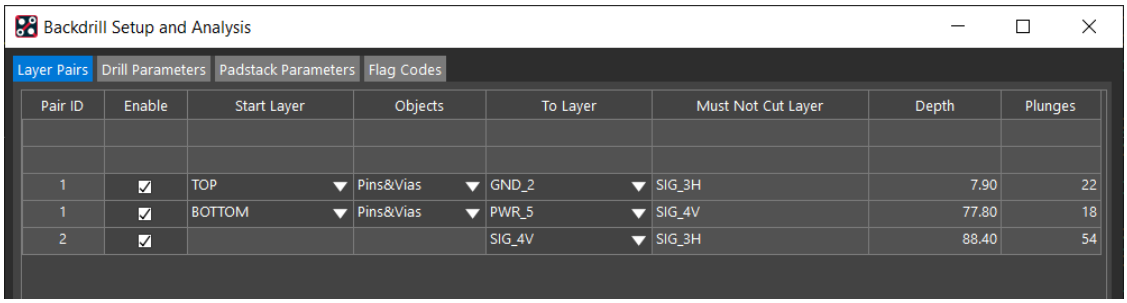


23. Restore the **Backdrill Setup and Analysis** form. Click the **Layer Pair Initialization** button.

24. In the **Backdrill Layer Pair Initialization** form, verify that **Minimize layer pairs** is selected, select **Create**, then select **Close**.



Now, there are only three backdrill layer pairs.



25. Click **OK** to close the form.

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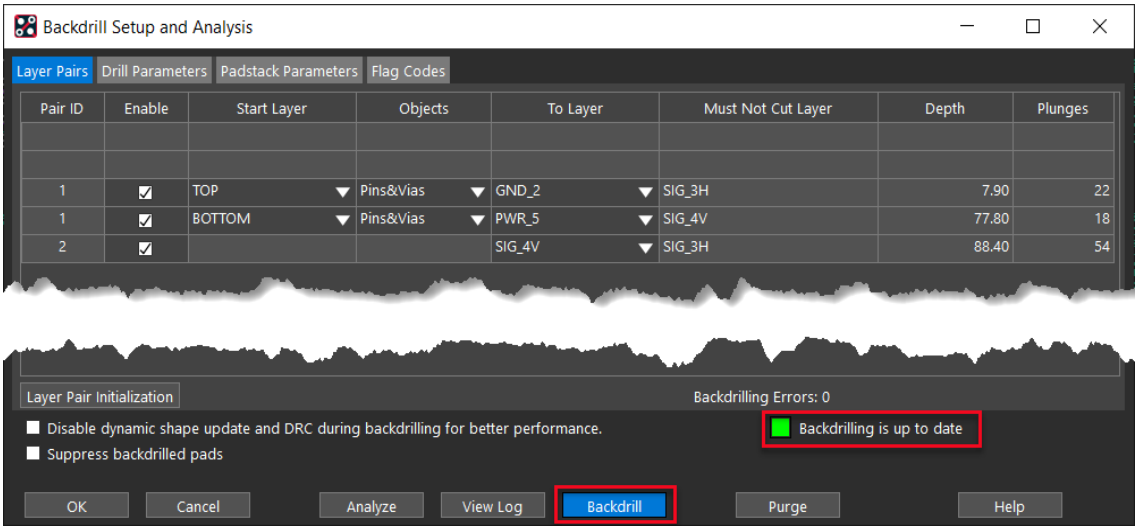
Lab 3: Processing and Saving Backdrill Data

1. Select **File > Open** and open **backdrill.brd**. You do not need to save any changes.

2. Select **Manufacture > NC > Backdrill Setup and Analysis**.

3. Select **Backdrill** in the **Backdrill Setup and Analysis** form. This will generate backdrill data on the pins and vias in the design.



The Backdrill status will turn green, indicating that the data on the pins and vias is up to date. If the backdrill data was out of date, the indicator would be red. If the indicator is gray, there is no backdrill data in the board.

4. Select **OK** to close the form.

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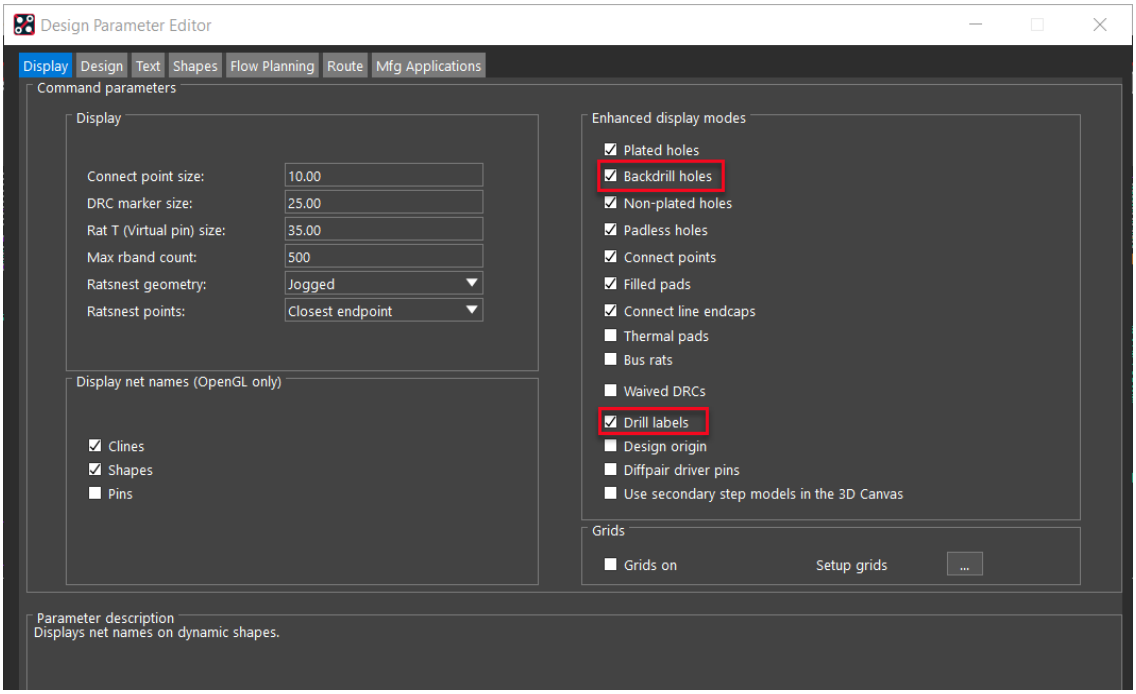
Lab 4: Canvas Display Controls

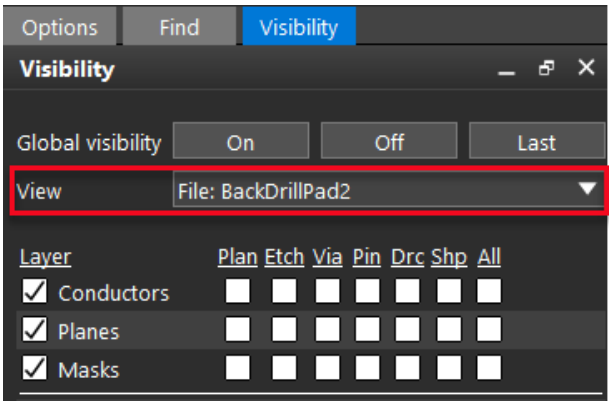
1. Select **Setup > Design Parameters**.

2. In the **Display** tab, check **Backdrill holes** and **Drill labels**. This will display the backdrill hole size and label on the Allegro canvas. The label is prefixed with the letter B, followed by the start layer, must cut layer, and must not cut layer.



3. Select **OK**.

4. Select the **BackDrillPad2** view from the **View** pulldown in the **Visibility** pane.



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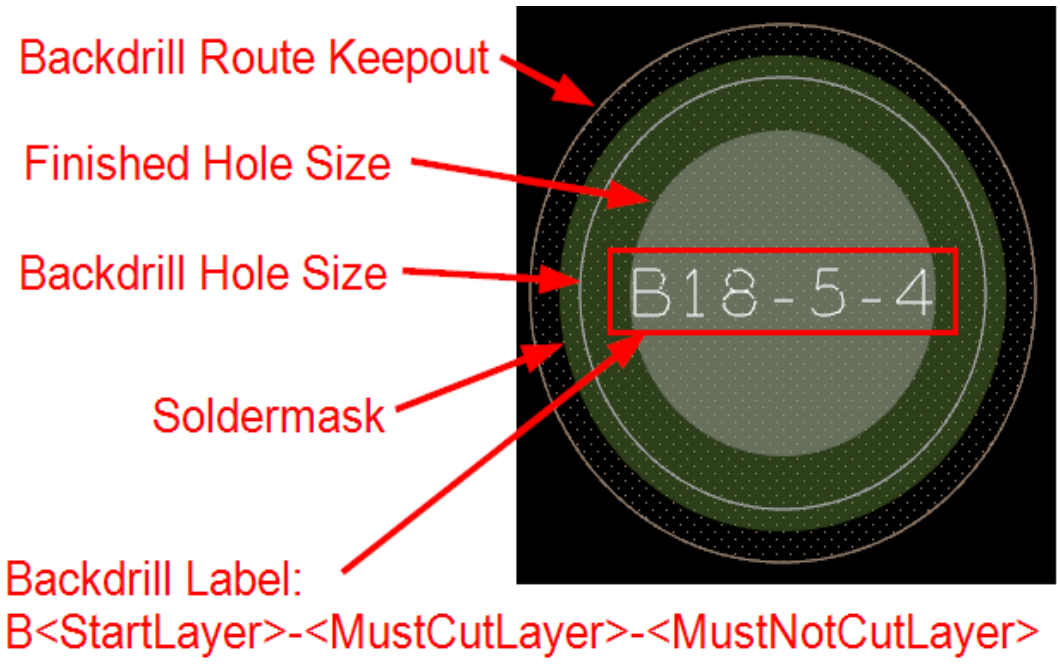
The following image shows the different elements of the backdrilled hole:



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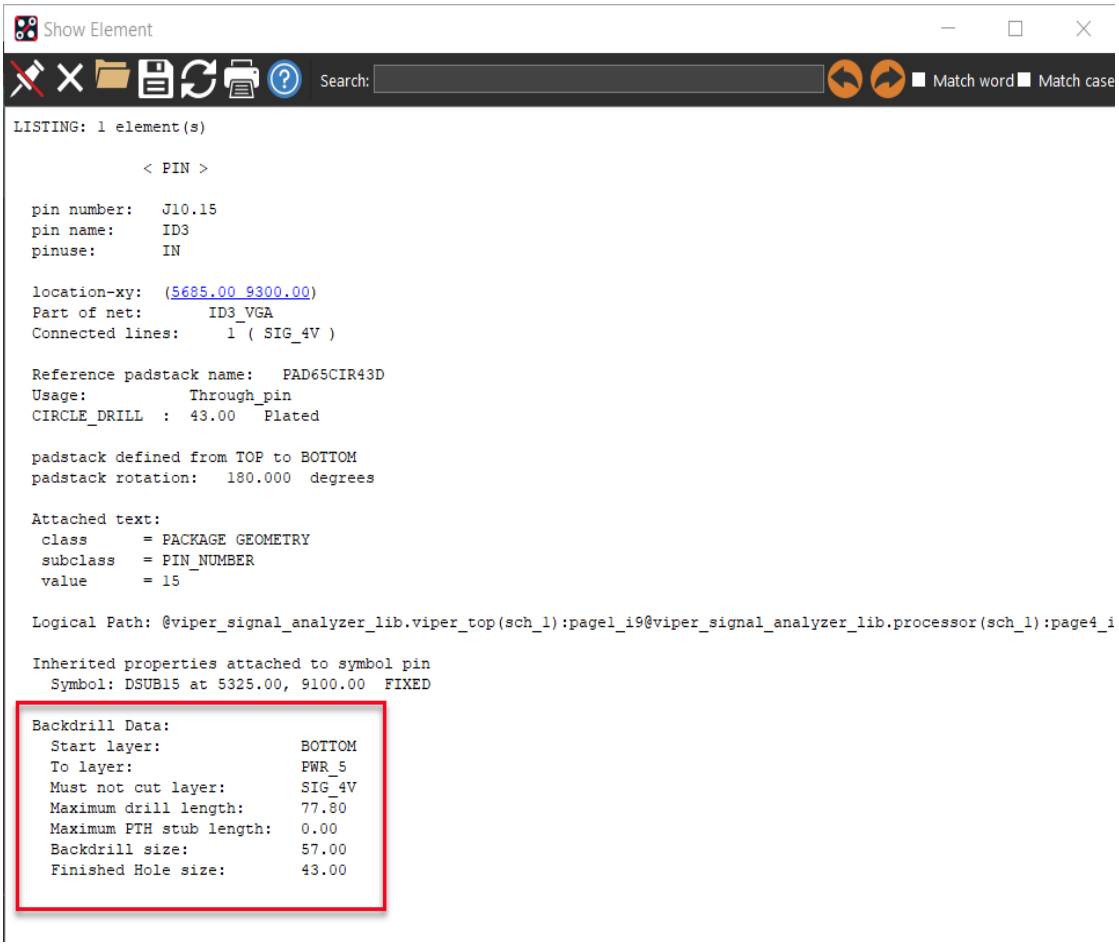
Lab 5: Displaying Backdrill Data Using Show Element

Backdrill data can also be reported on individual pins or vias using **Show Element**.

1. Select **Display > Element**.
2. In the **Find** filter, select **All Off**, then select **Pins**.
3. Click on a backdrill pin. Review the backdrill information.



4. Close the **Show Element** window.

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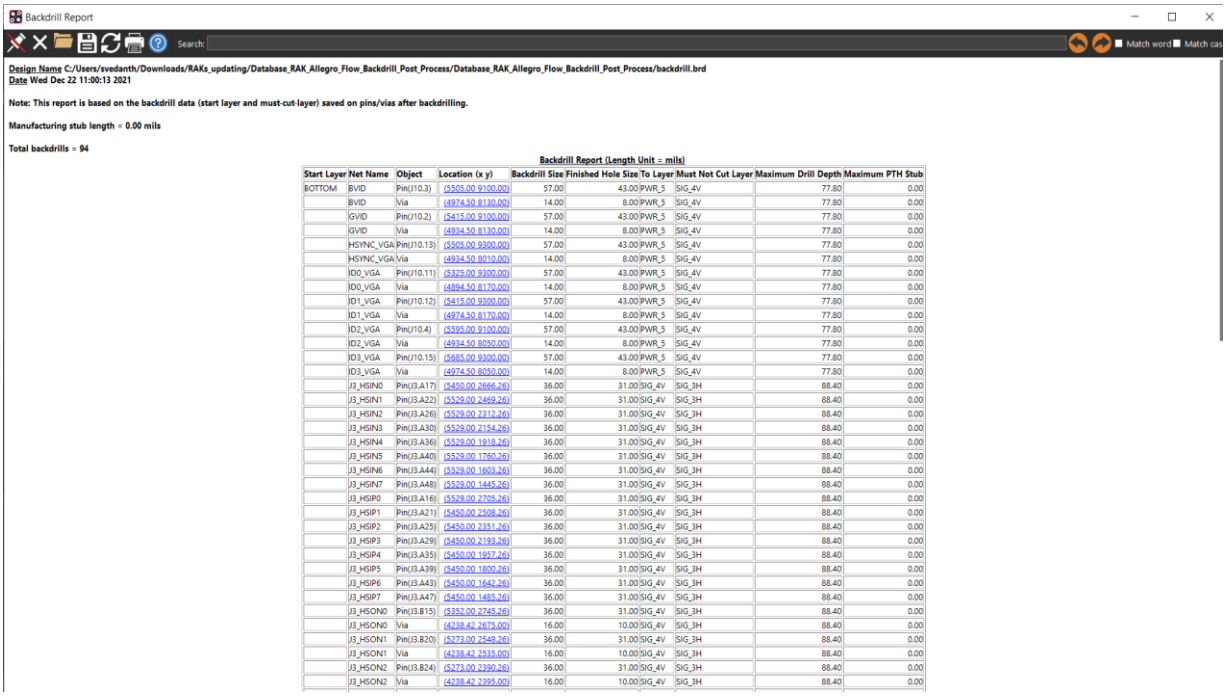
Lab 6: Backdrill Report Support

A **Backdrill Report** can be generated to list all backdrill data for the backdrilled pins and vias, including the manufacturing stub lengths. To generate the report, select **Tools > Quick Reports > Backdrill**.


Backdrill Report

Search:

Match word Match cas

Design Name C:/Users/svedanth/Downloads/RAKs_updating/Database_RAK_Allegro_Flow_Backdrill_Post_Process/Database_RAK_Allegro_Flow_Backdrill_Post_Process/backdrill.brd
Date Wed Dec 22 11:00:13 2021

Note: This report is based on the backdrill data (start layer and must-cut-layer) saved on pins/vias after backdrilling.

Manufacturing stub length = 0.00 mils

Total backdrills = 94

Backdrill Report (Length Unit = mils)

Start Layer	Net Name	Object	Location (x y)	Backdrill Size	Finished Hole Size	To Layer	Must Not Cut Layer	Maximum Drill Depth	Maximum PTH Stub
BOTTOM	BVID	Pin(J10.3)	(5505.00 9100.00)	57.00	43.00	PWR_5	SIG_4V	77.80	0.00
	BVID	Via	(4974.50 8130.00)	14.00	8.00	PWR_5	SIG_4V	77.80	0.00
	GVID	Pin(J10.2)	(5415.00 9100.00)	57.00	43.00	PWR_5	SIG_4V	77.80	0.00
	GVID	Via	(4934.50 8130.00)	14.00	8.00	PWR_5	SIG_4V	77.80	0.00
	HSYNC_VGA	Pin(J10.13)	(5505.00 9300.00)	57.00	43.00	PWR_5	SIG_4V	77.80	0.00
	HSYNC_VGA	Via	(4934.50 8010.00)	14.00	8.00	PWR_5	SIG_4V	77.80	0.00
	ID0_VGA	Pin(J10.11)	(5325.00 9300.00)	57.00	43.00	PWR_5	SIG_4V	77.80	0.00
	ID0_VGA	Via	(4894.50 8170.00)	14.00	8.00	PWR_5	SIG_4V	77.80	0.00
	ID1_VGA	Pin(J10.12)	(5415.00 9300.00)	57.00	43.00	PWR_5	SIG_4V	77.80	0.00
	ID1_VGA	Via	(4974.50 8170.00)	14.00	8.00	PWR_5	SIG_4V	77.80	0.00
	ID2_VGA	Pin(J10.4)	(5595.00 9100.00)	57.00	43.00	PWR_5	SIG_4V	77.80	0.00
	ID2_VGA	Via	(4934.50 8050.00)	14.00	8.00	PWR_5	SIG_4V	77.80	0.00
	ID3_VGA	Pin(J10.15)	(5685.00 9300.00)	57.00	43.00	PWR_5	SIG_4V	77.80	0.00
	ID3_VGA	Via	(4974.50 8050.00)	14.00	8.00	PWR_5	SIG_4V	77.80	0.00
	J3_HSIN0	Pin(J3.A17)	(5450.00 2666.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSIN1	Pin(J3.A22)	(5529.00 2469.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSIN2	Pin(J3.A26)	(5529.00 2312.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSIN3	Pin(J3.A30)	(5529.00 2154.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSIN4	Pin(J3.A36)	(5529.00 1918.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSIN5	Pin(J3.A40)	(5529.00 1760.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSIN6	Pin(J3.A44)	(5529.00 1603.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSIN7	Pin(J3.A48)	(5529.00 1445.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSIP0	Pin(J3.A16)	(5529.00 2705.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSIP1	Pin(J3.A21)	(5450.00 2508.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSIP2	Pin(J3.A25)	(5450.00 2351.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSIP3	Pin(J3.A29)	(5450.00 2193.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSIP4	Pin(J3.A35)	(5450.00 1957.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSIP5	Pin(J3.A39)	(5450.00 1800.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSIP6	Pin(J3.A43)	(5450.00 1642.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSIP7	Pin(J3.A47)	(5450.00 1485.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSON0	Pin(J3.B15)	(5352.00 2745.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSON0	Via	(4238.42 2675.00)	16.00	10.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSON1	Pin(J3.B20)	(5273.00 2548.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSON1	Via	(4238.42 2535.00)	16.00	10.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSON2	Pin(J3.B24)	(5273.00 2390.26)	36.00	31.00	SIG_4V	SIG_3H	88.40	0.00
	J3_HSON2	Via	(4238.42 2395.00)	16.00	10.00	SIG_4V	SIG_3H	88.40	0.00

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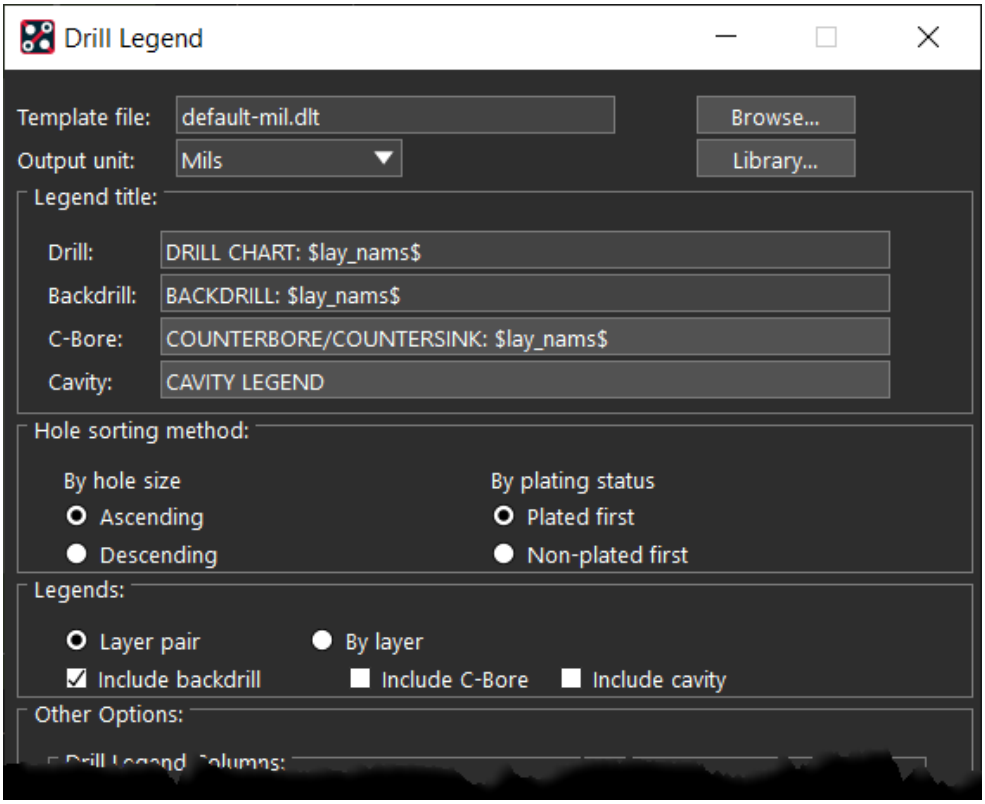
Lab 7: Backdrill NC Drill Legend and Cross Section Chart Display

Backdrill information can be included on the NC drill legend and in the Cross Section detail.

1. Select **Manufacture > NC > Drill Legend**.
2. Enable the **Include backdrill** option.



3. Click **OK** to generate the backdrill legends, which include detailed backdrill information.

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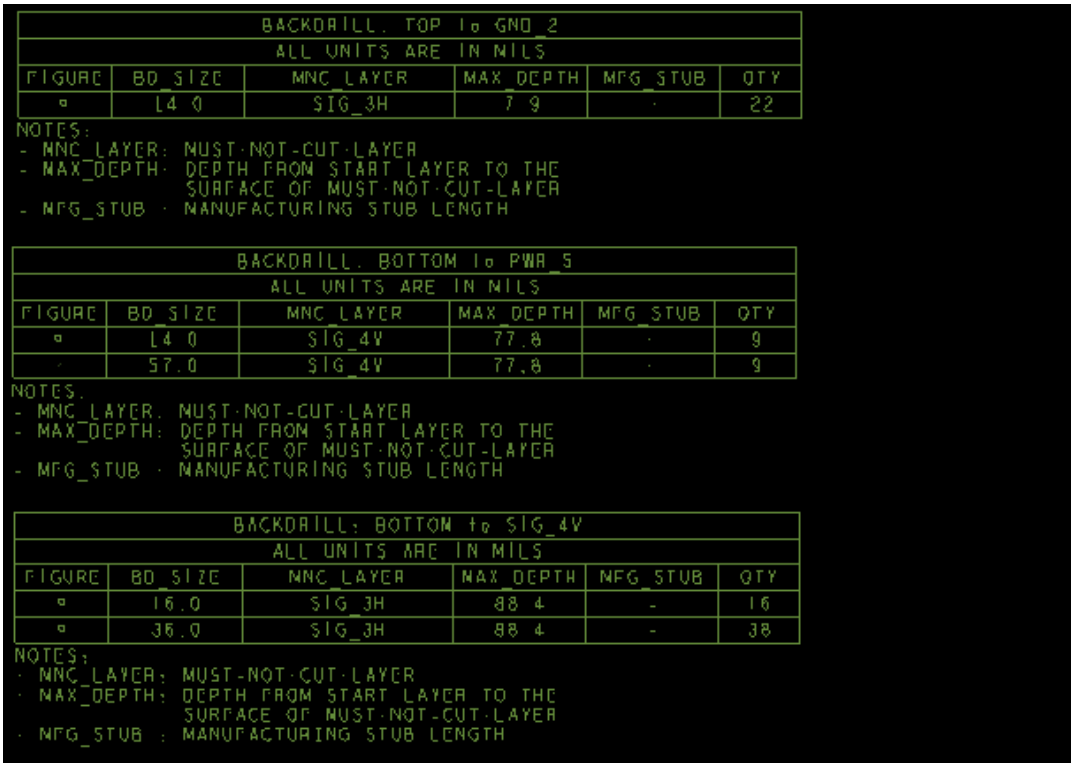
4. Place the legends anywhere on the design. There are three backdrill legends generated – TOP to GND_2, BOTTOM to PWR_5, and BOTTOM to SIG_4V.



BACKDRILL. TOP to GND_2
ALL UNITS ARE IN MILS

FIGURE	BD_SIZE	MNC_LAYER	MAX_DEPTH	MFG_STUB	QTY
▫	14.0	SIG_3H	7.9	.	22

NOTES:
- MNC_LAYER: MUST-NOT-CUT-LAYER
- MAX_DEPTH: DEPTH FROM START LAYER TO THE SURFACE OF MUST-NOT-CUT-LAYER
- MFG_STUB : MANUFACTURING STUB LENGTH

BACKDRILL. BOTTOM to PWR_5
ALL UNITS ARE IN MILS

FIGURE	BD_SIZE	MNC_LAYER	MAX_DEPTH	MFG_STUB	QTY
▫	14.0	SIG_4V	77.8	.	9
.	57.0	SIG_4V	77.8	.	9

NOTES.
- MNC_LAYER. MUST-NOT-CUT-LAYER
- MAX_DEPTH: DEPTH FROM START LAYER TO THE SURFACE OF MUST-NOT-CUT-LAYER
- MFG_STUB : MANUFACTURING STUB LENGTH

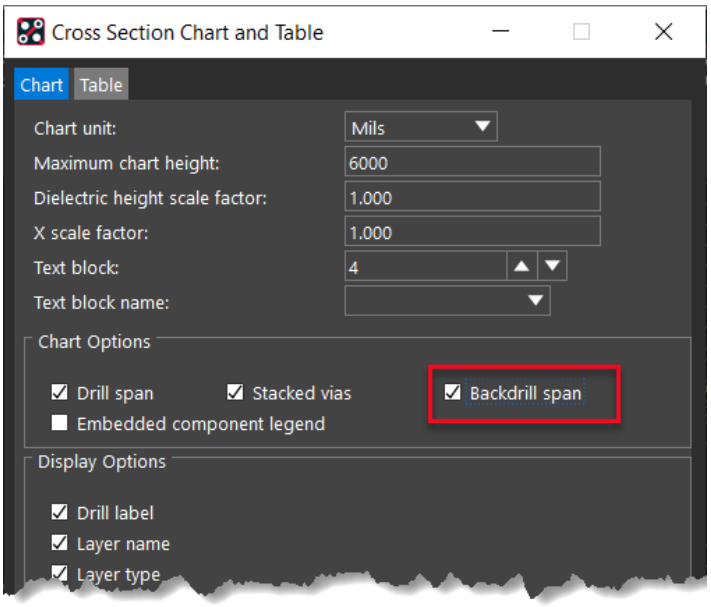
BACKDRILL: BOTTOM to SIG_4V
ALL UNITS ARE IN MILS

FIGURE	BD_SIZE	MNC_LAYER	MAX_DEPTH	MFG_STUB	QTY
▫	16.0	SIG_3H	88.4	-	16
▫	36.0	SIG_3H	88.4	-	38

NOTES:
- MNC_LAYER: MUST-NOT-CUT-LAYER
- MAX_DEPTH: DEPTH FROM START LAYER TO THE SURFACE OF MUST-NOT-CUT-LAYER
- MFG_STUB : MANUFACTURING STUB LENGTH

5. To generate **Cross Section Chart**, select **Manufacture > Cross Section Chart**.

6. Enable **Backdrill span**.



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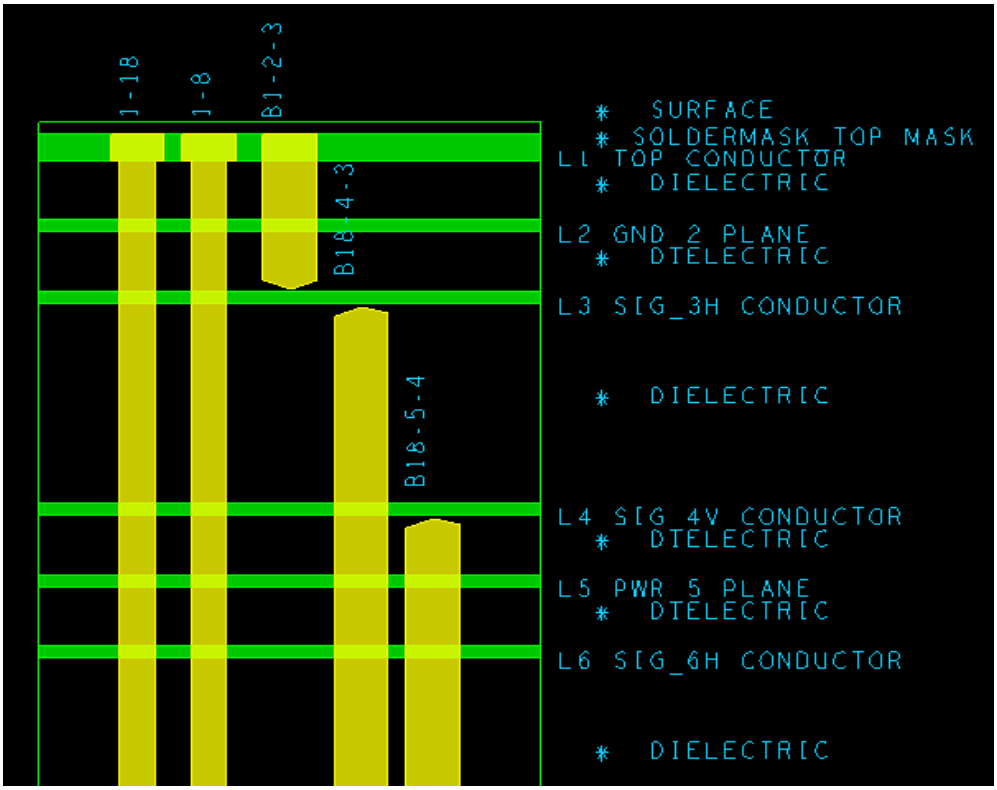
7. Click **OK**. **Cross Section Chart** will be attached to the cursor.

8. Place the chart anywhere on the canvas. The backdrilled holes are displayed with tapered ends and backdrill labels.



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Module 2: Post-Processing

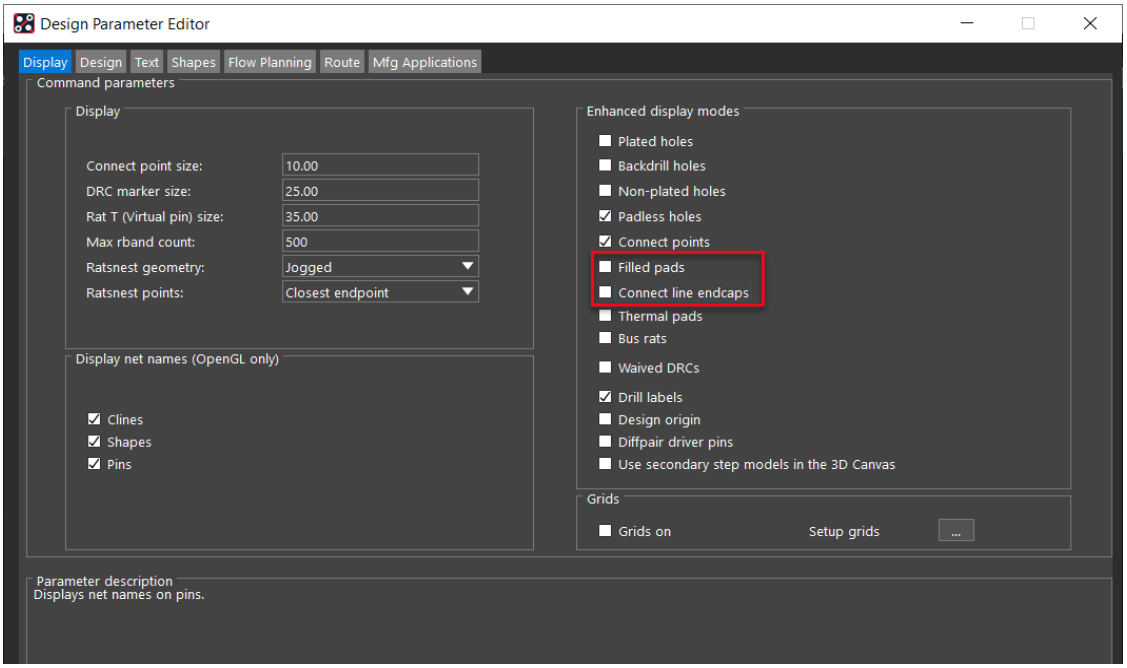
Once the board is routed, it is ready for post-processing. This can include generating:

- testpoints,
- drill customization,
- cross section chart and table,
- artwork, and thieving.

Lab 8: Testpoint Generation Using Testprep

Testprep creates test probe sites for any type of test fixture. Testpoints can be created automatically or interactively, and testpoint locations can be edited. Once testpoints are generated, artwork and NC data files can be created for drilling design test beds.

1. Open **fab.brd** in Allegro PCB Editor. You do not need to save the design.
2. Select **Setup > Design Parameters**.
3. In the **Display** tab, uncheck **Filled pads** and **Connect line endcaps**.



This will turn off the enhanced display mode (which fills pads solid) so that the testpoint symbols are easier to see.

4. Select **OK**.
5. Select **Manufacture > Testprep > Automatic**.

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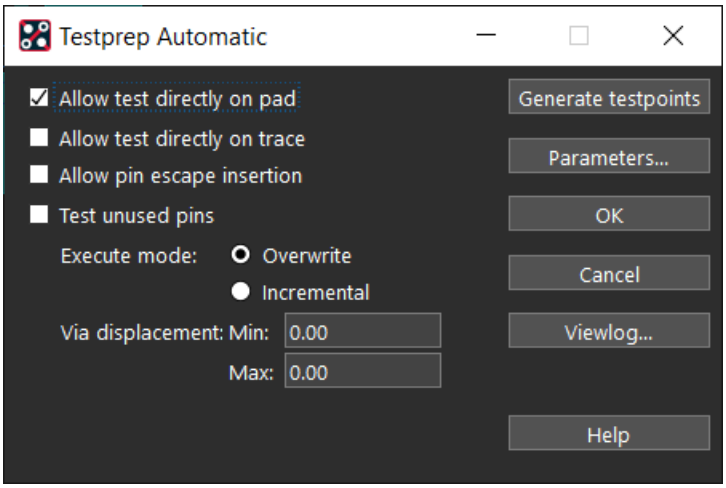
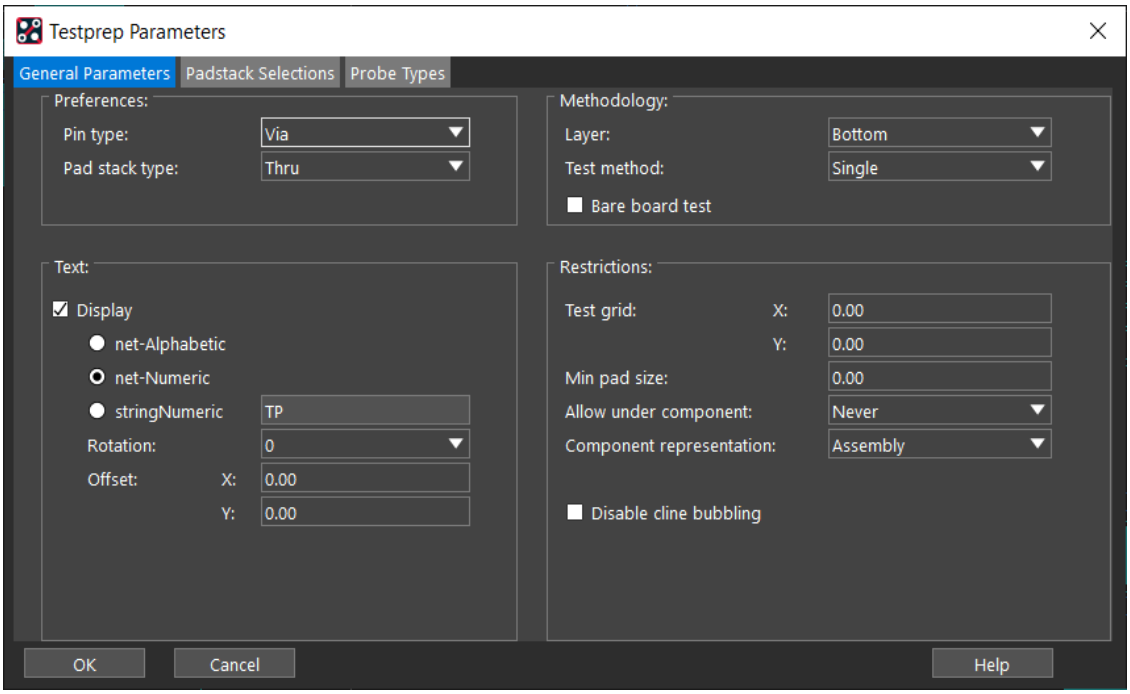
6. Set the form as shown below:



These settings allow testpoints to be selected from the existing pad locations and not add any more pads or vias.

7. Select the **Parameters** button.

8. Set the **Testprep Parameter** form to test an assembled board, as shown below:



9. Click **OK**.

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10. Click **Generate Testpoints** in the **Testprep Automatic** form. This will start the execution of the Testprep process.

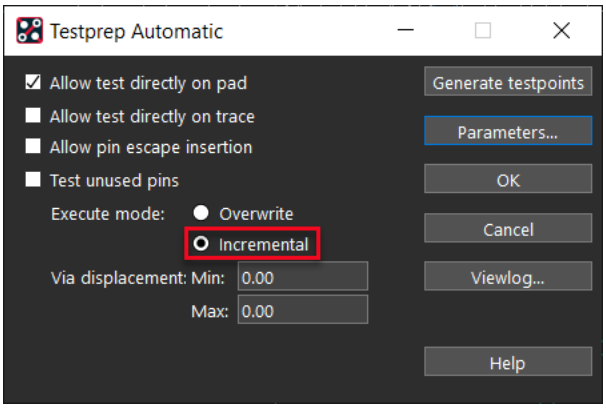
11. Zoom in to see the sites marked as probe points. As the Testprep program selects sites as probe points, it marks each site with a white triangle (indicating a bottom-side testpoint).

12. Click **Viewlog** from the **Testprep Automatic** form to view the log file. This displays the net name and coordinates of all test probe locations as well as a list of nets that failed to receive a testpoint location.

    For example, if it was unable to access a net from the back side of the board, the program has run out of legal vias to select. The next steps will automatically add testpoints to through-hole pins on the bottom of the board.

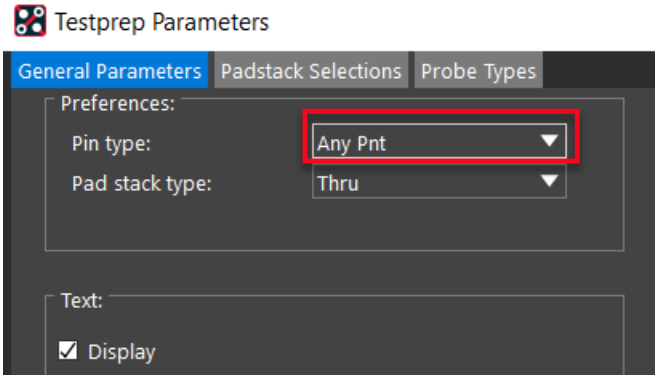
13. Close the log file.

14. In the **Testprep Automatic** form, change the **Execute mode** to **Incremental**.



15. Select **Parameters**.

16. Change the **Pin Type** to **Any Pnt** and click **OK**.



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17. Select **Generate testpoints** to run Testprep. Notice that testpoints have now been added to through-hole pins in addition to the vias.

18. Select **OK** in the **Testprep Automatic** form to exit Testprep.

19. To create a test fixture drill file, select **Manufacture > Testprep > Create NC drill data**. The editor command-line area reports the following:

```
Probe drill file creation complete.
```


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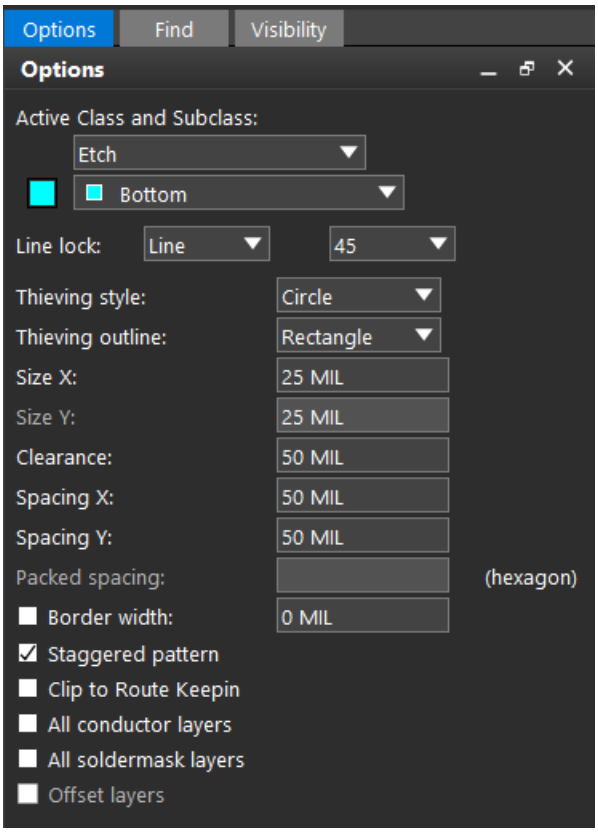
Lab 9: Thieving

The thieving command lets you add a pattern of non-conductive, single-layer figures to areas on the outer layers of a physical design that do not contain copper. The thieving pattern is generated to balance the plating distribution, placing it to avoid interference with the signal quality of adjacent circuits. Use thieving near the end of the design process, prior to artwork generation.

This lab will outline how to add thieving to the bottom layer.

1. Reopen **fab.brd**. You do not need to save the changes that were made.
2. Select **Manufacture > Thieving**.
3. Set the options shown below in the **Options** pane:



   This will place a staggered array of 25 mil circular surface mount vias 50 mils apart.

4. Draw a rectangle around an area of the BOTTOM layer. The thieving will be added inside this rectangular area.

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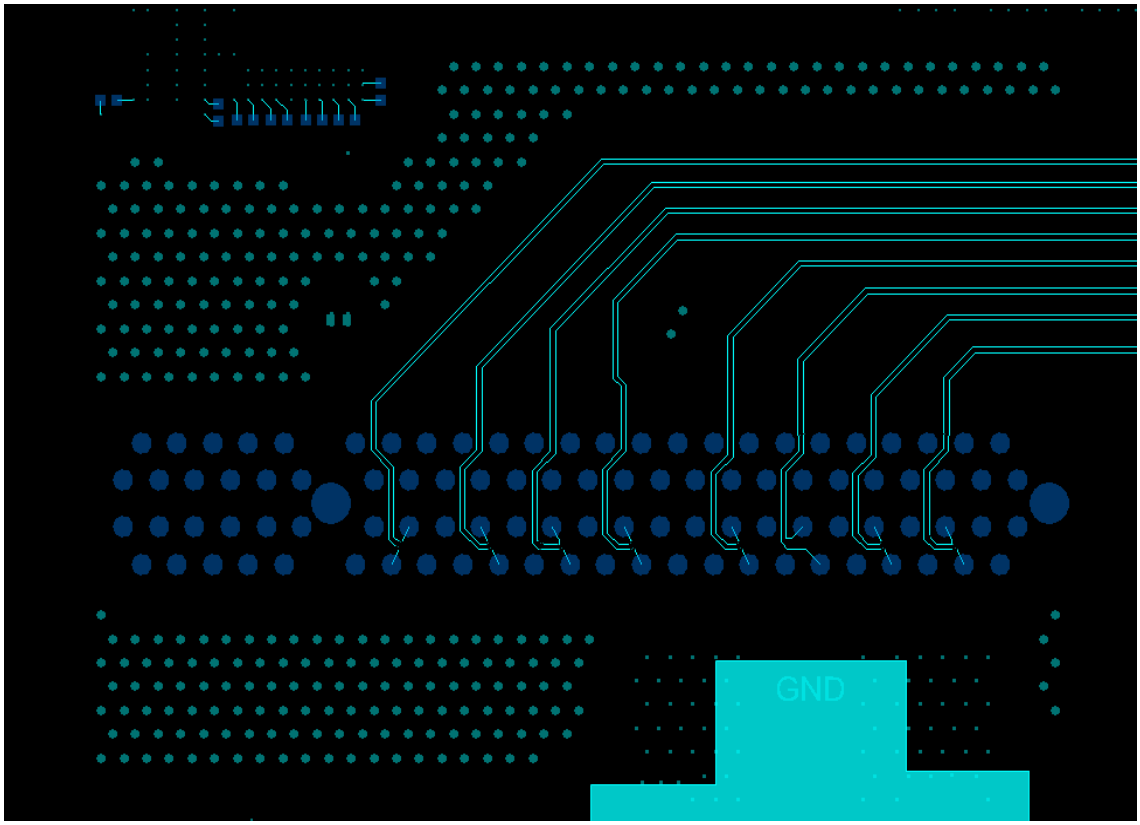
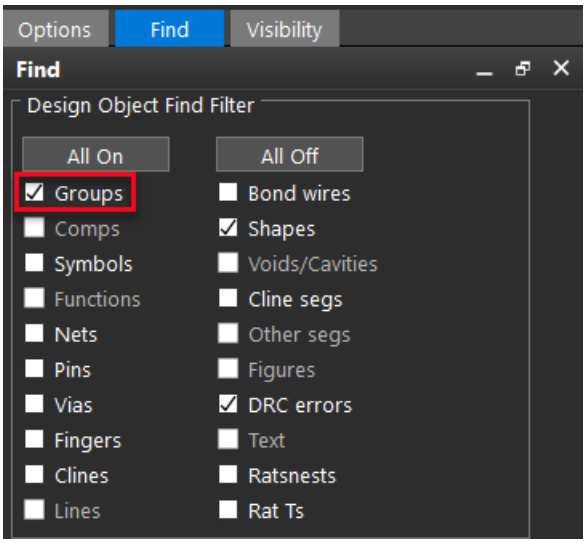


5. Right-click in the canvas and select **Done**.

6. Since thieving is added as a group of vias, it can easily be deleted. Turn on **Groups** in the **Find** filter.



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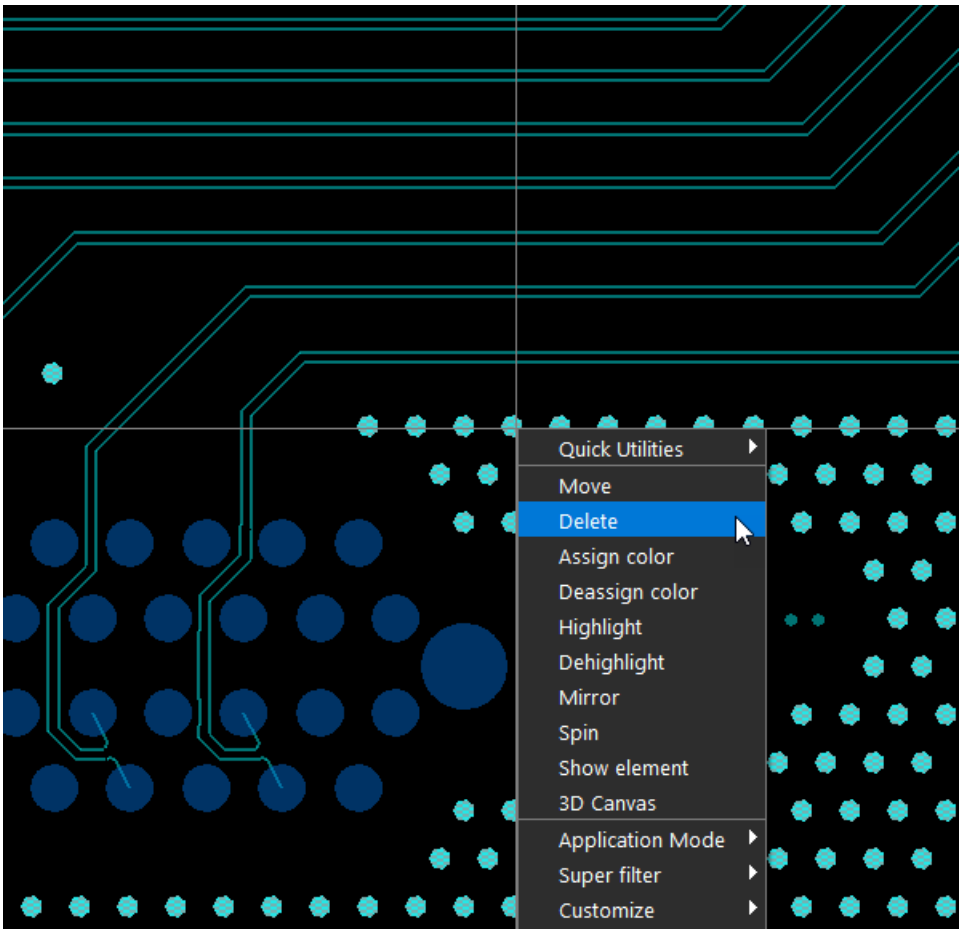
7. Right-click on any of the thieving vias and select **Delete**.



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Lab 10: NC Drill Legend Creation

During the last phase of PCB design, drill legend tables are created, which usually appear on a fabrication drawing, quantifying the number, type, and tolerance of plated and non-plated holes. These tables are automatically created when you run the **ncdrill legend** command.

1. Open **start.brd** in Allegro PCB Designer.

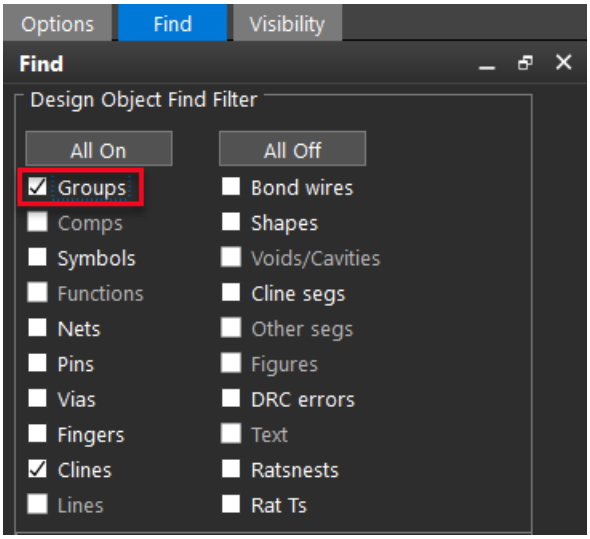
2. Select **Manufacture > NC > Drill Legend**.

   Cadence supplies template files to control the drill legend table format and let you customize its appearance. The drill template file specifies the number and order of columns, column titles, and custom data for each tool size in the design. Since the database units are mils, the template file named *default-mil.dlt* is being used.

3. Click **OK** in the **Drill Legend** form to generate the drill legend.

4. Place the legends anywhere in the design. Notice that there are multiple drill legends placed on top of each other (TOP to BOTTOM and TOP to PWR_8). Each legend is generated as a group and can easily be moved once it is placed.

5. In the **Find** filter, turn on **Groups**.



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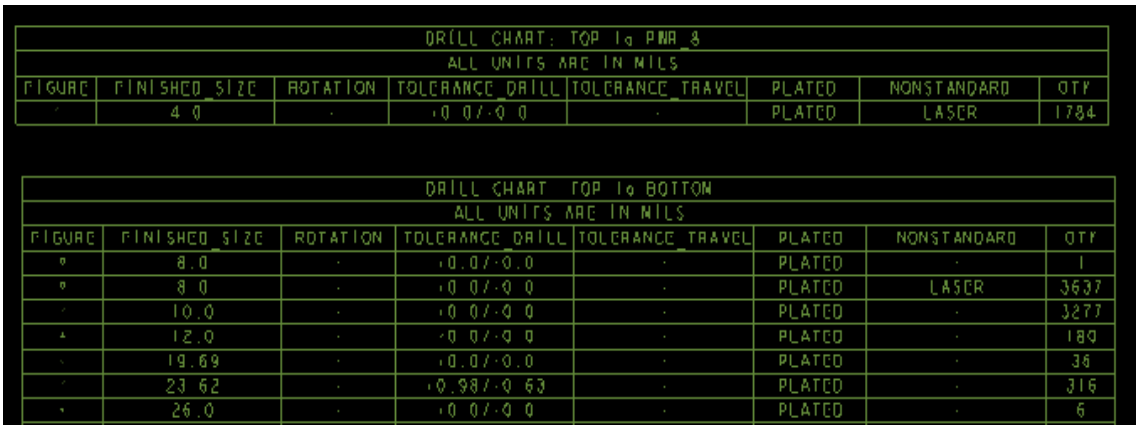
6. Right-click on the legends and select **Move**. Place the legend on a different part of the drawing. You can now see each individual legend.



DRILL CHART: TOP to PWA_8
ALL UNITS ARE IN MILS

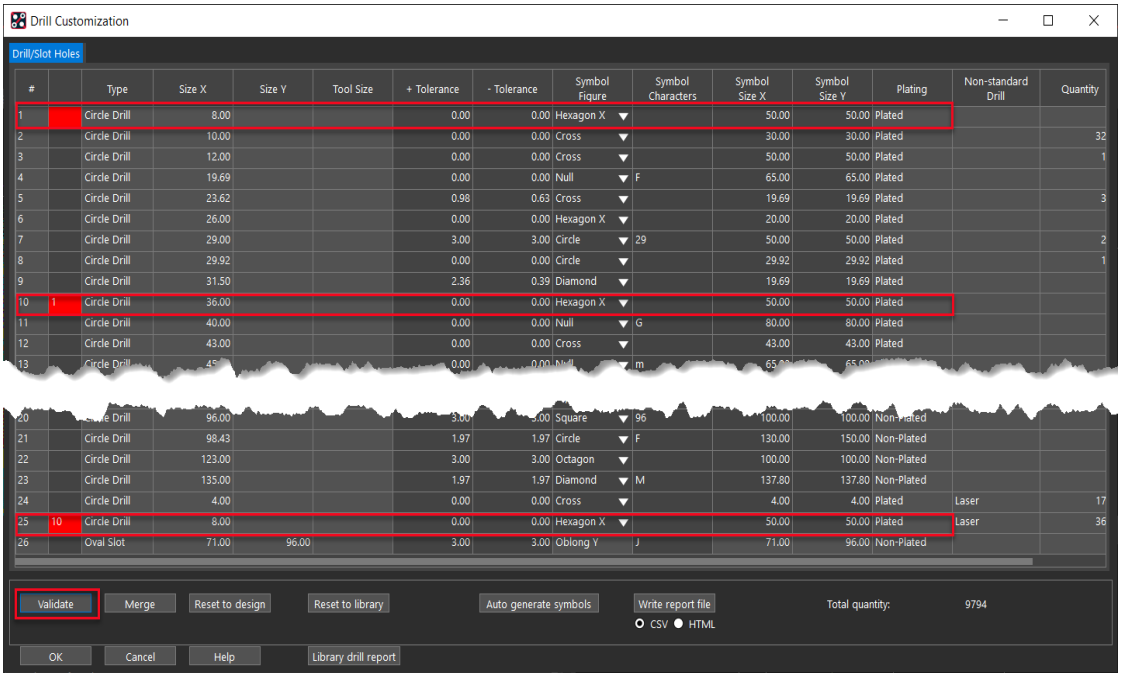
FIGURE	FINISHED_SIZE	ROTATION	TOLERANCE_DRILL	TOLERANCE_TRAVEL	PLATED	NONSTANDARD	QTY
	4.0		+0.0/-0.0		PLATED	LASER	1784

DRILL CHART TOP to BOTTOM
ALL UNITS ARE IN MILS

FIGURE	FINISHED_SIZE	ROTATION	TOLERANCE_DRILL	TOLERANCE_TRAVEL	PLATED	NONSTANDARD	QTY
	8.0		+0.0/-0.0		PLATED		1
	8.0		+0.0/-0.0		PLATED	LASER	3637
	10.0		+0.0/-0.0		PLATED		3277
	12.0		+0.0/-0.0		PLATED		180
	19.69		+0.0/-0.0		PLATED		38
	23.62		+0.98/-0.63		PLATED		316
	26.0		+0.0/-0.0		PLATED		6

7. Select **Manufacture > NC > Drill Customization**.

8. Click **Validate**. The red boxes indicate that there is a conflict in drill definitions. The drill figures for drills 1, 10, and 25 are all defined as a 50 mil Hexagon X.



#		Type	Size X	Size Y	Tool Size	+ Tolerance	- Tolerance	Symbol Figure	Symbol Characters	Symbol Size X	Symbol Size Y	Plating	Non-standard Drill	Quantity
1		Circle Drill	8.00			0.00	0.00	Hexagon X		50.00	50.00	Plated		
2		Circle Drill	10.00			0.00	0.00	Cross		30.00	30.00	Plated		32
3		Circle Drill	12.00			0.00	0.00	Cross		50.00	50.00	Plated		1
4		Circle Drill	19.69			0.00	0.00	Null	F	65.00	65.00	Plated		
5		Circle Drill	23.62			0.98	0.63	Cross		19.69	19.69	Plated		3
6		Circle Drill	26.00			0.00	0.00	Hexagon X		20.00	20.00	Plated		
7		Circle Drill	29.00			3.00	3.00	Circle	29	50.00	50.00	Plated		2
8		Circle Drill	29.92			0.00	0.00	Circle		29.92	29.92	Plated		1
9		Circle Drill	31.50			2.36	0.39	Diamond		19.69	19.69	Plated		
10	1	Circle Drill	36.00			0.00	0.00	Hexagon X		50.00	50.00	Plated		
11		Circle Drill	40.00			0.00	0.00	Null	G	80.00	80.00	Plated		
12		Circle Drill	43.00			0.00	0.00	Cross		43.00	43.00	Plated		
13		Circle Drill	45			0.00	0.00	Null	m	65.00	65.00			
20		Circle Drill	96.00			3.00	3.00	Square	96	100.00	100.00	Non-Plated		
21		Circle Drill	98.43			1.97	1.97	Circle	F	130.00	150.00	Non-Plated		
22		Circle Drill	123.00			3.00	3.00	Octagon		100.00	100.00	Non-Plated		
23		Circle Drill	135.00			1.97	1.97	Diamond	M	137.80	137.80	Non-Plated		
24		Circle Drill	4.00			0.00	0.00	Cross		4.00	4.00	Plated	Laser	17
25	10	Circle Drill	8.00			0.00	0.00	Hexagon X		50.00	50.00	Plated	Laser	36
26		Oval Slot	71.00	96.00		3.00	3.00	Oblong Y	J	71.00	96.00	Non-Plated		

9. Change the **Symbol Figure** for drill **10** to **Triangle** and the **Symbol Size X/Y** to **75/75**. Add **Tolerance** of **+/- 3**.

10. Change the **Symbol Figure** for drill **1** to **Circle** and the **Symbol Size X/Y** to **75/75**. Notice that any customizations appear in blue.

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Drill/Slot Holes

#		Type	Size X	Size Y	Tool Size	+ Tolerance	- Tolerance	Symbol Figure	Symbol Characters	Symbol Size X	Symbol Size Y	Plat
1		Circle Drill	8.00			0.00	0.00	Circle		75	75	Plated
2		Circle Drill	10.00			0.00	0.00	Cross		30.00	30.00	Plated
3		Circle Drill	12.00			0.00	0.00	Cross		50.00	50.00	Plated
4		Circle Drill	19.69			0.00	0.00	Null	F	65.00	65.00	Plated
5		Circle Drill	23.62			0.98	0.63	Cross		19.69	19.69	Plated
6		Circle Drill	26.00			0.00	0.00	Hexagon X		20.00	20.00	Plated
7		Circle Drill	29.00			3.00	3.00	Circle	29	50.00	50.00	Plated
8		Circle Drill	29.92			0.00	0.00	Circle		29.92	29.92	Plated
9		Circle Drill	31.50			2.36	0.39	Diamond		19.69	19.69	Plated
10		Circle Drill	36.00			3	3	Triangle		75	75	Plated
11		Circle Drill	40.00			0.00	0.00	Null	G	80.00	80.00	Plated
12		Circle Drill	43.00			0.00	0.00	Cross		43.00	43.00	Plated

11. Click **Validate**. There are no longer any conflicts between the drill symbols.

12. Click **OK** to close the **Drill Customization** form. Click **Yes** in the confirmation dialog that appears. This will update the padstacks in the design with the changed drill information.

13. Select **Manufacture > NC > Drill Legend**.

14. Select **OK** in the **Drill Legend** form and place the legends. Notice that the TOP to BOTTOM drill chart has been updated with the customized drill information.

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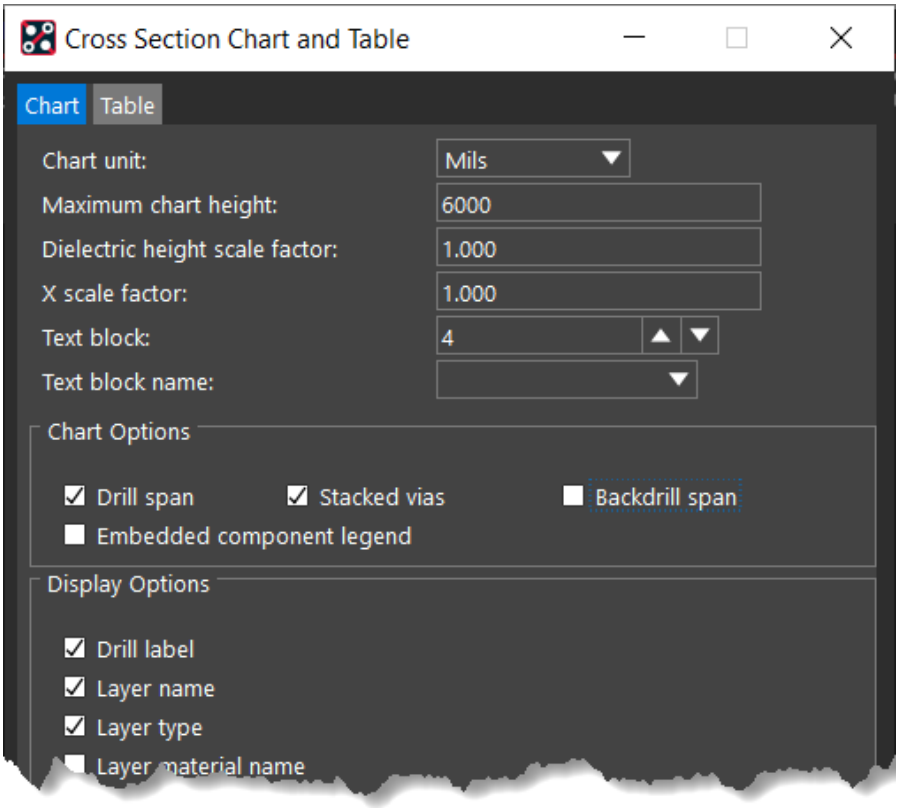
Lab 11: Cross Section Chart and Table Creation

A detailed view of the cross section can be generated, displaying the drill span, stacked vias, embedded component legend, and layer information. Like the NC Drill Legend, the chart is registered as a group object and will retain its current position upon recursive outputs. You can also create the cross-section information in a table format.

1. Continue using **start.brd**.
2. Select **Manufacture > Cross Section Chart**.
3. Change **Maximum chart height** to **6000** and **Text block** to **4**.



4. Select **OK** and place the chart on the canvas.
5. Select **Manufacture > Cross Section Chart**.
6. Select the **Table** tab.
7. Change the **Text block** to **3**.
8. Select **OK** and place the table on the canvas.

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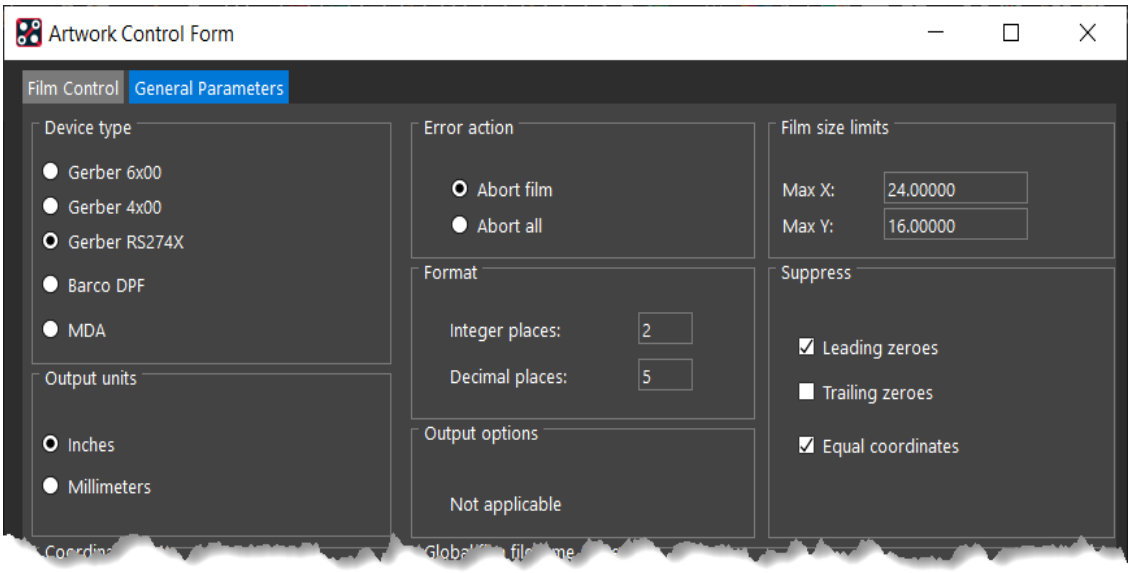
Lab 12: Generating Artwork Files

Artwork files or Gerber files are some of the most important items required to manufacture a printed circuit board. To generate the artwork files, film records must exist within the design. The records identify where all data resides for each artwork file to be created. These records are stored internally in the database.

The *art_param.txt* file must exist in the ARTPATH. This file contains all parameters used when creating artwork.

1. Open **fab.brd**. You do not need to save any changes.
2. Select **Manufacture > Artwork**.
3. Select the **General Parameters** tab in **Artwork Control Form**. This form specifies the plotter type, film size, and format of the manufacturing data.
4. Verify that the following parameters are set. Then, select **OK** to close the form.



When **Artwork Control Form** is closed, the parameter settings are written in the working directory to a file named *art_param.txt*.

Each layer for which you want to create artwork must be entered in the **Artwork Film Control** table. By default, Allegro PCB Editor will create a film control record for each of the etch subclasses in the design.

5. Select **Manufacture > Artwork**. The **Film Control** tab specifies which artwork files are to be created and which objects in the database make up each artwork file.

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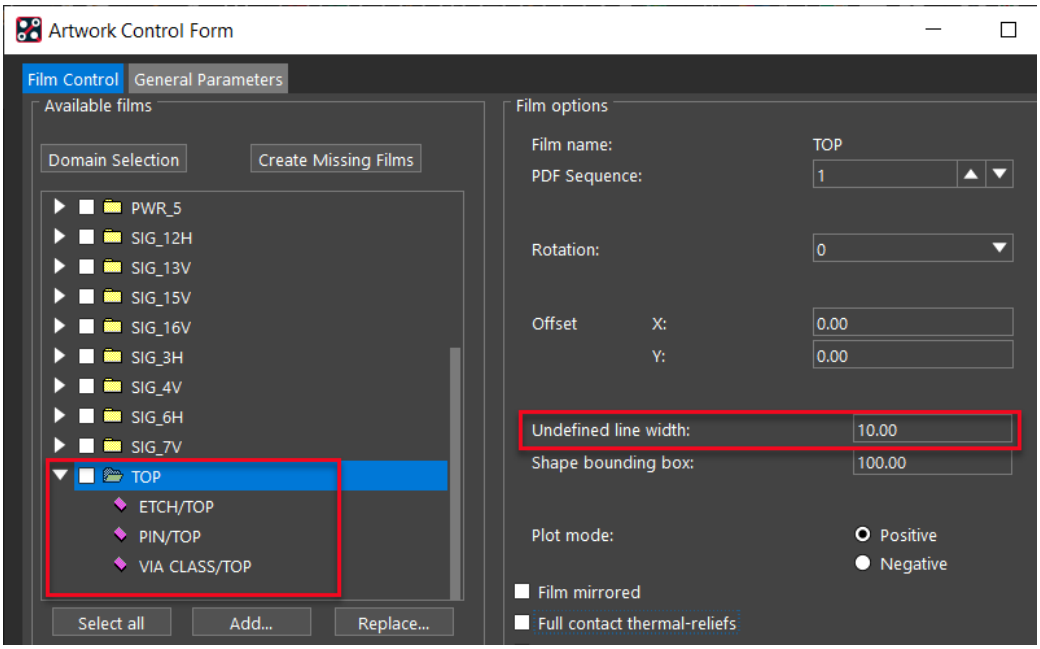
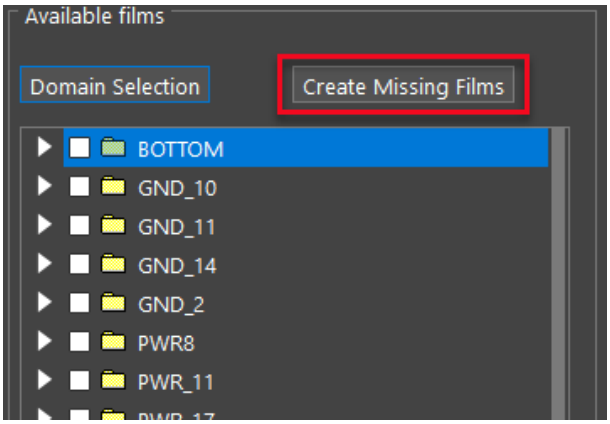
6. Click the **>** sign next to the **TOP** entry in the **Available films** section. The TOP film control record expands to display the class/subclass entries that will be included in the manufacturing file for this artwork film. By default, Allegro PCB Editor includes the ETCH, PIN, and VIA class for each of the etch subclasses.

7. Set the **Undefined line width** to **10**.



8. Select **Create Missing Films**. This button will be active if the layout stackup does not match the artwork stackup.



In this case, there are only film control records for the etch layers, but the stackup includes soldermask layers.

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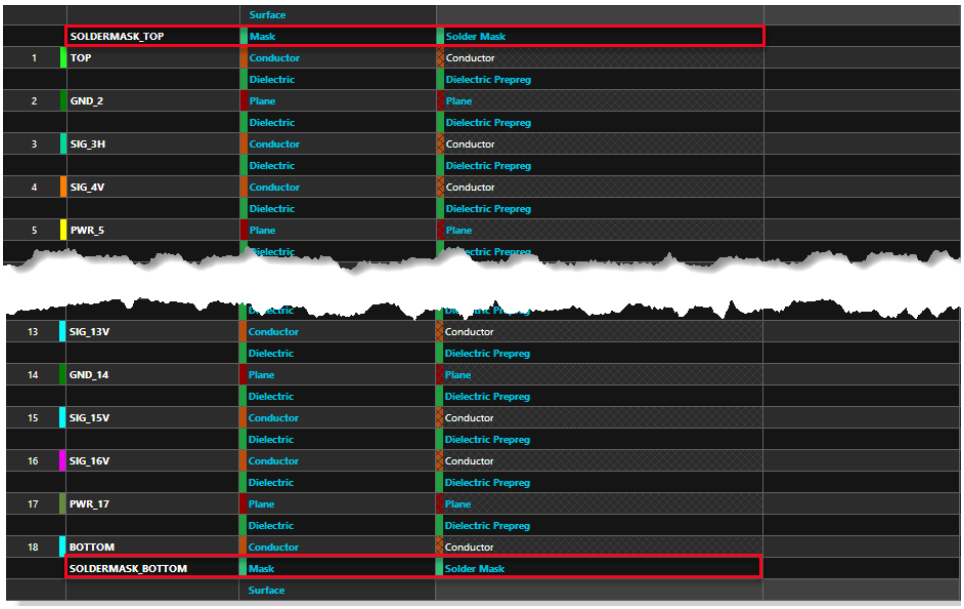
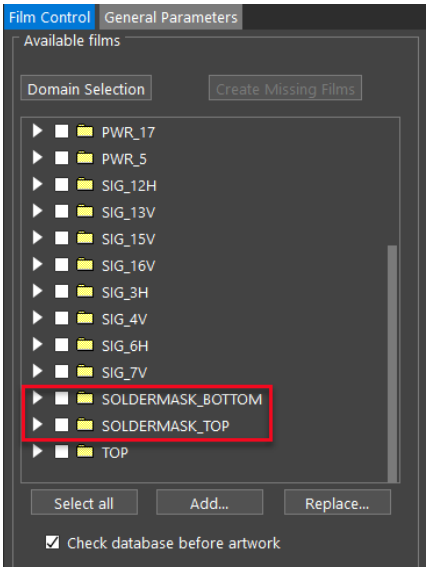


Notice that the soldermask film control records have been created.



Artwork files need to be created for other non-etch layers, such as top and bottom silkscreen. A film control record must be created for each of these layers. By default, when a new film control record is created, all currently visible classes and subclasses are added to the film control record.

9. To create an artwork file for the top silkscreen layer, select **Display > Color/Visibility** from the Allegro PCB Editor menu.

   Note: Do not close the **Artwork Control Form** window.

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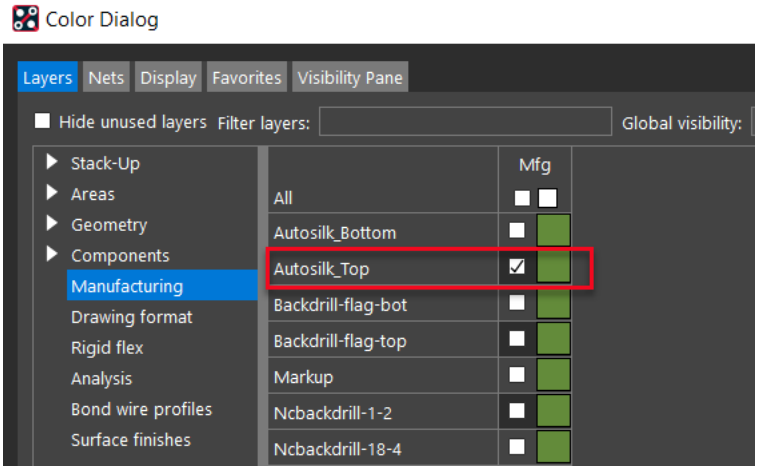
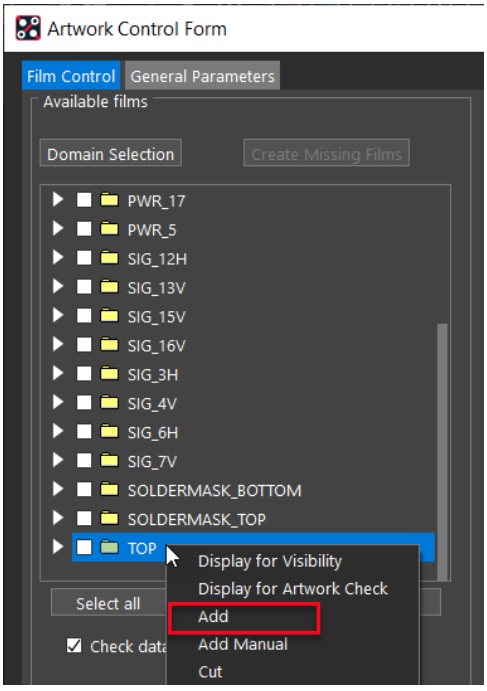
10. Click the **Global Visibility Off** button to turn off all classes and subclasses.

11. Click on the **Manufacturing** group.

12. Turn on the **AUTOSILK_TOP** subclass to redisplay the color settings. Leave the **Color Dialog** window open.



13. In the **Available films** section of **Artwork Control Form**, right-click on **TOP** and select **Add**. A form opens, asking for the name of the new film.



14. Enter a name of **SILKSCREEN_TOP** and click **OK**.

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15. Set the **Undefined Line Width** to **10** in the **Film Options** section of **Artwork Control Form**.

16. In **Color Dialog**, turn off **AUTOSILK_TOP** and turn on **AUTOSILK_BOTTOM**.

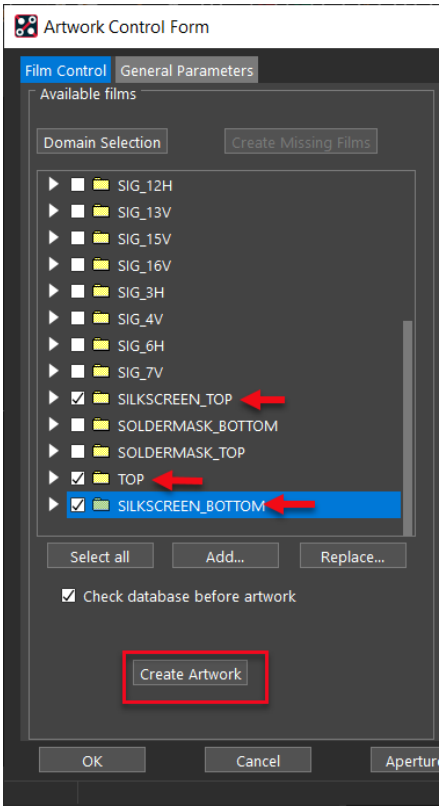
17. Click **OK** in **Color Dialog**.

18. In the **Available films** section of **Artwork Control Form**, right-click on **SILKSCREEN_TOP** and select **Add**. A form opens, asking for the name of the new film.

19. Enter the name as **SILKSCREEN_BOTTOM** and click **OK**.

20. Set the **Undefined Line Width** to **10** in the **Film Options** section of **Artwork Control Form**.

21. Check the boxes next to **TOP**, **SILKSCREEN_TOP**, and **SILKSCREEN_BOTTOM**. Then, select **Create Artwork**.



This will generate files named *TOP.art*, *SILKSCREEN_TOP.art*, and *SILKSCREEN_BOTTOM* in the working directory.

22. Select **OK** in **Artwork Control Form**.

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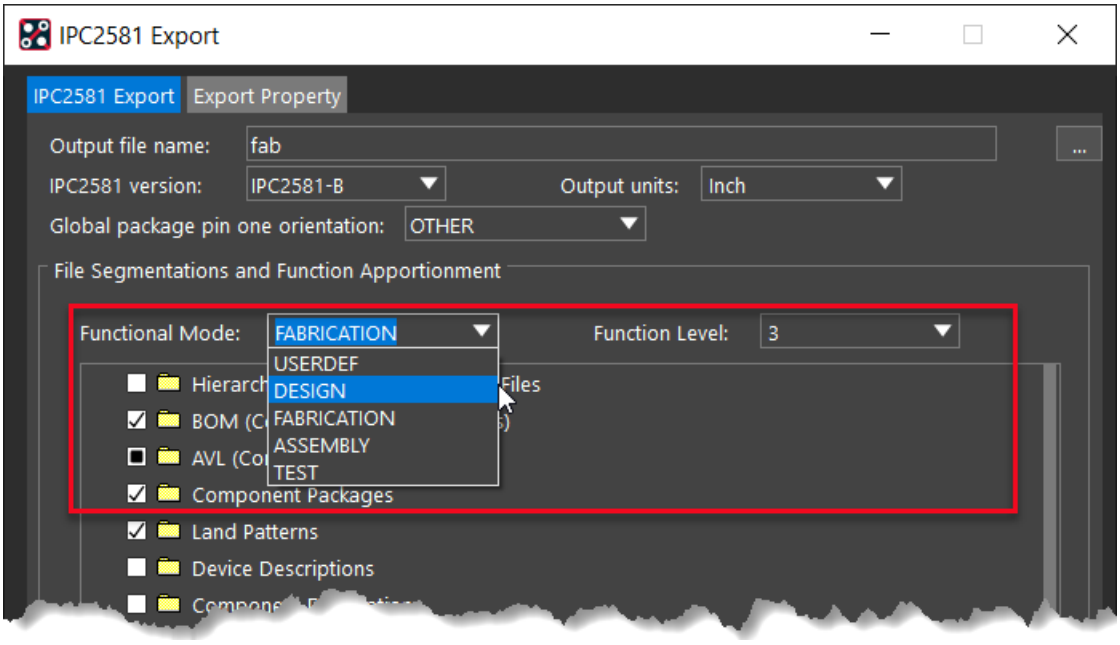
Lab 13: IPC-2581 Export

IPC-2581 is an open standard supported and managed by IPC. This standard provides a single XML-formatted data file for the exchange of PCB design data from ECAD tools to manufacturing processes.

The export of IPC-2581 begins from a completed design with artwork film records defined for the export of conductor layers, masks, and drawings.

The **File Segmentations and Function Apportionment** section defines what data is to be exported from the design database. IPC-2581 export lets you export all design data or select only the data relative to a particular environment. For example, board fabrication data may not be required for an assembly facility, so the board fabrication data can be excluded.

The IPC-2581 specification defines five specific modes for export, each with different levels of data. As each function is selected, and each level within each function, the data item list is changed based on what the IPC-2581 standard has defined. You may also select and unselect any of the options in the data export list to control data extraction.



Layer Mapping Editor defines film layers as specific data types required by IPC-2581. These data type associations are used with the format for clarification of film layer intent when imported into other IPC-2581 tools. The data types distinguish between copper, masking, and documentation layers.

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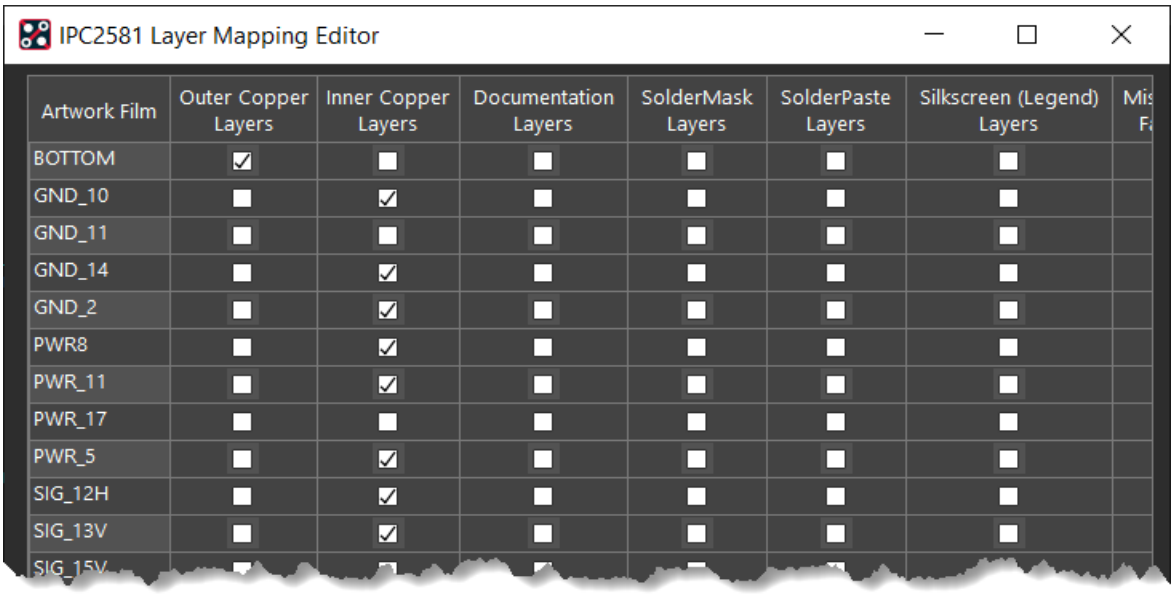
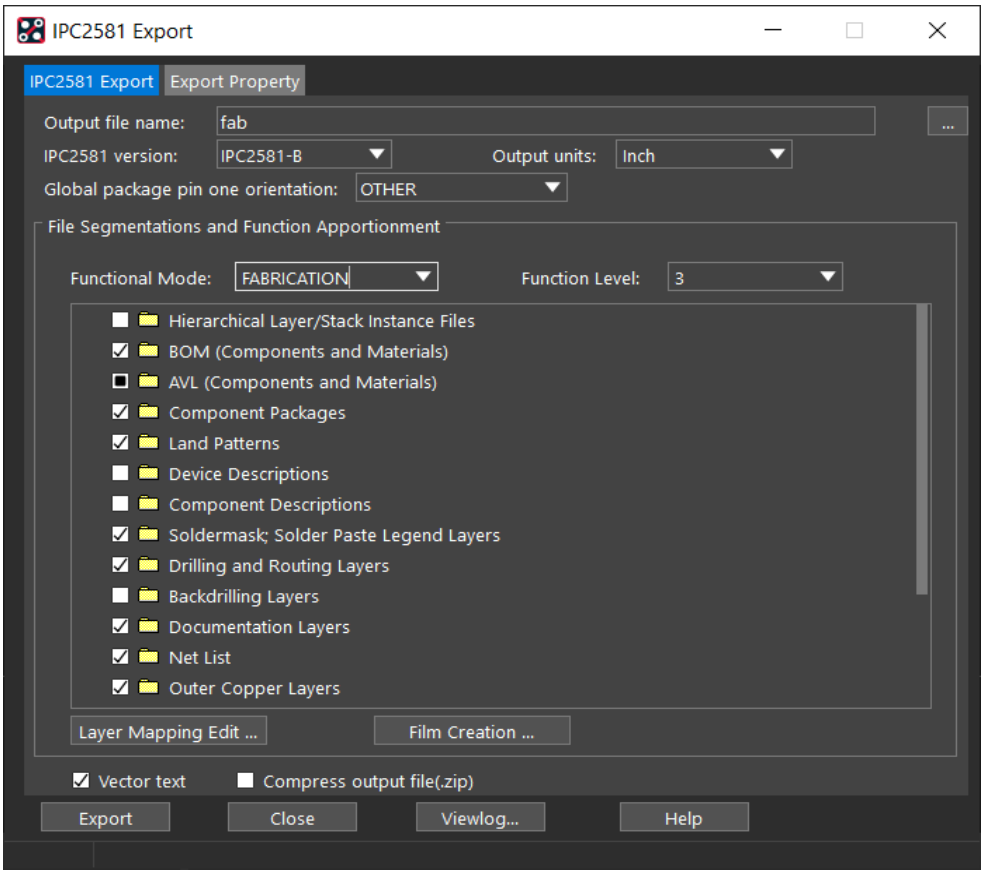


1. In Allegro PCB Editor, select **File > Export > IPC 2581**.
2. Set the form fields as shown below:



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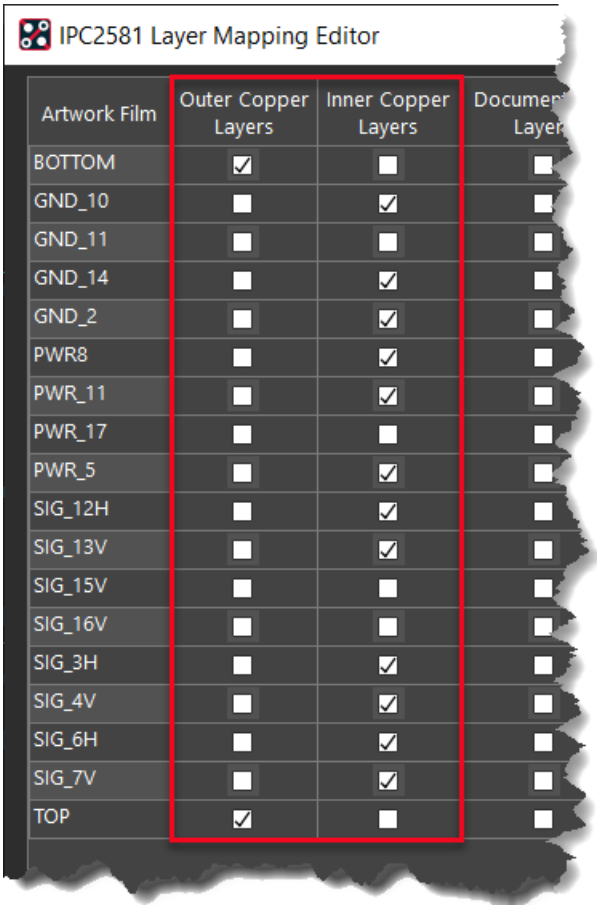
3. Select **Layer Mapping Edit**.

4. Select **Outer Copper Layers** and **Inner Layers** as shown below. Then, click **OK** to close the form.



5. Select **Export** to create the IPC-2581 file.

6. Close the **IPC2581 Export** form and the **ipc2581_out.log** window.

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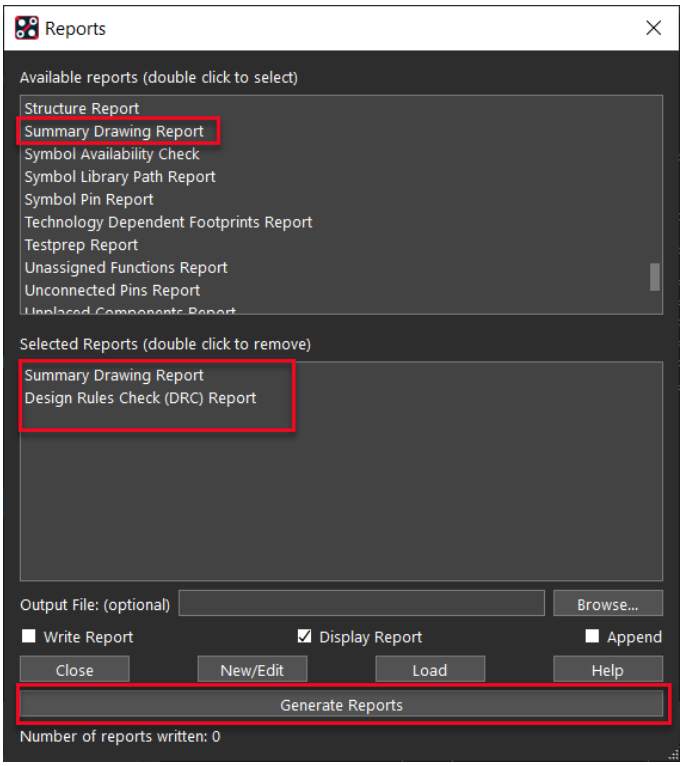
Lab 14: Report Generation

Allegro PCB Editor provides many predefined reports that can be run from within the current design. The **Tools > Reports** command opens the **Reports** form, which lets you generate multiple reports simultaneously or you can use **Tools > Quick Reports** to quickly generate a single report.

1. Continue in **fab.brd**.
2. Select **Tools > Reports**. Scroll through the list of **Available reports**.
3. Double-click on **Design Rules Check (DRC) Report** and **Summary Drawing Report**. These reports will be added to the list of **Selected Reports**.



4. Select **Generate Reports**. The reports will open in separate windows.
5. Close the **Reports** form and both report windows.
6. Single reports can be generated without using the **Reports** form. Select **Tools > Quick Reports > Summary Drawing Report** to display **Summary Drawing Report**.
7. Exit Allegro PCB Editor. You do not need to save the drawing. This completes the RAK.

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