cādence

Design Authoring and PSpice Basic Analysis

Rapid Adoption Kit (RAK)

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Copyright Statement

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Purpose

The purpose of this RAK is to guide you through the process of creating a design using OrCAD Capture and then simulating the design using PSpice. You will discover the power of this full-featured analog and mixed-signal simulator, which supports everything from high-frequency systems to low-power IC designs.

Audience

This document is intended for analog design engineers who are interested in performing board-level SPICE analysis of their designs. Knowledge of basic analog simulation is recommended.

Overview

Filters, amplifiers, linear and switched-mode power supplies, and other linear and mixed-signal designs require rigorous verification and analysis to ensure that they will perform to their design specifications. Failures and yield problems due to violations of component safe operating limits, component value (or parameter) variation, or the fact the design was just not optimized, all lead to increased cost and schedule slippage. The PSpice simulator is ideally suited to address these issues via its user-friendly interface and extensive suite of Advanced Analysis features.

Through a combination of lecture and hands-on material, you will be introduced to schematic entry, simulation, stress analysis, design optimization, and yield analysis using Cadence PSpice Simulator and the OrCAD Capture editor. You will discover the power of this full-featured analog and mixed-signal simulator, which supports everything from high-frequency systems to low-power IC designs.

Throughout this workshop, **PSpice Simulator** and **OrCAD Capture** will often be referred to as **PSpice** and **Capture**, respectively. PSpice and its supporting tools, such as the Model Editor and Advanced Analysis tools, may be seen with the name AMS Model Editor and AMS Advanced Analysis as PSpice is also part of the Allegro product line.

Module 1: Design Authoring Using OrCAD Capture

- New Project Creation
- Vendor Part Import
- Tool Configuration
- Schematic Entry

Start Capture by selecting the Windows **Start** icon and selecting **All Programs > Cadence Release SPB 17.2-2016 > Capture CIS or Cadence PCB 17.4-2019 > Capture CIS 17.4**.

If prompted, select **OrCAD PSpice Designer Plus** as the product. This determines which license is used by Capture, as well as which Design Authoring tool will be used. The Capture window appears.

Figure 1-1: OrCAD Capture

This is the Capture Start page. From here, you can open previous designs or start new designs.

Lab 1: Creating a New Project

In this section, you will create a new project.

1. Select **File > New > Project** to bring up the **New Project** wizard.

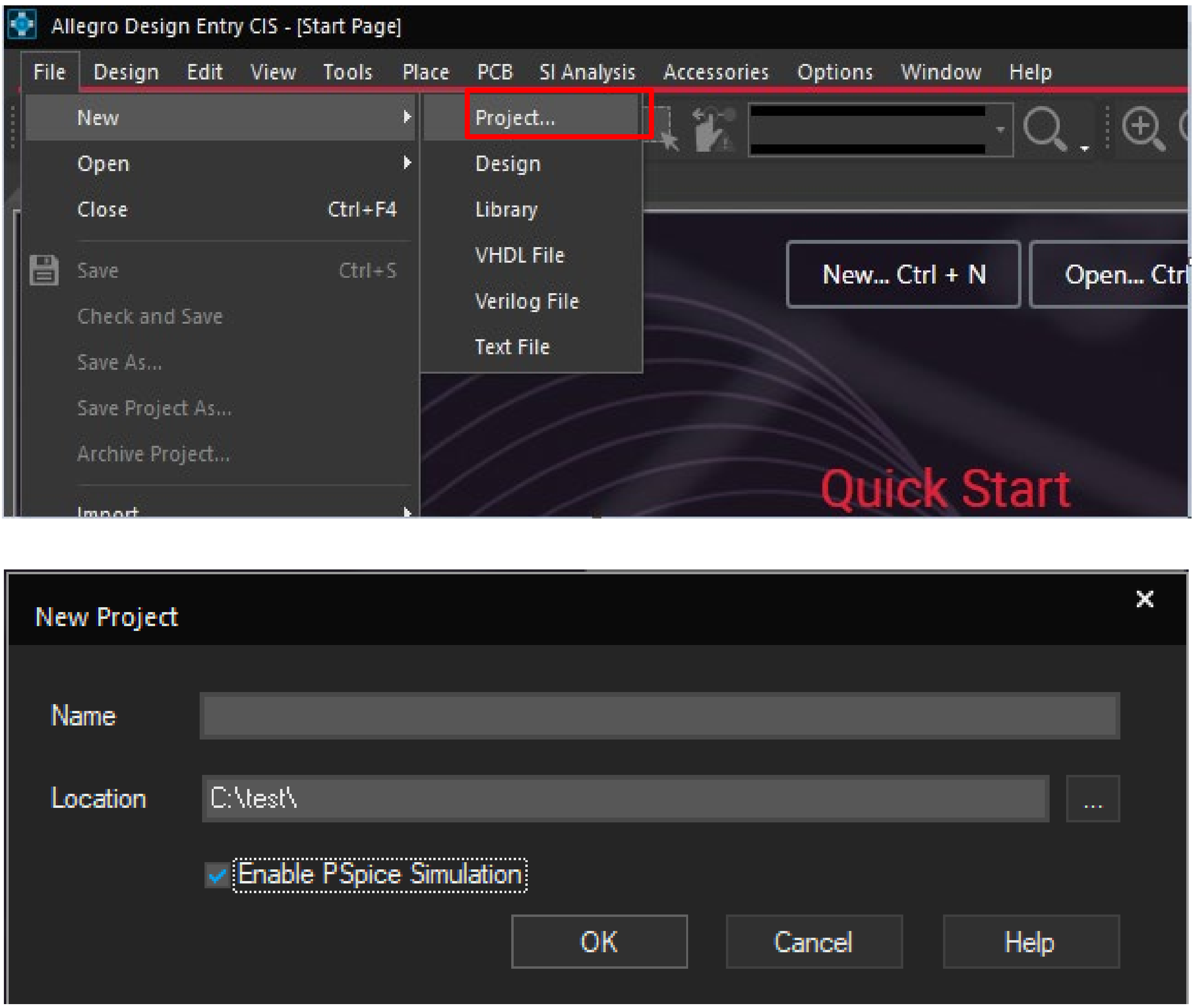


Figure 1-2: New Project creation wizard

You will create a simple common-emitter amplifier. The project will be named “amp”. Project names in Capture use mixed-case characters and numbers.

2. Enter amp in the **Name** field, as shown in Figure 1-3.

3. In the **Location** field, select the **Ellipsis** button (**…**) and browse to the **C:\Workshops\PSpice\PSpice_Basic_Simulation\Lab1** folder.

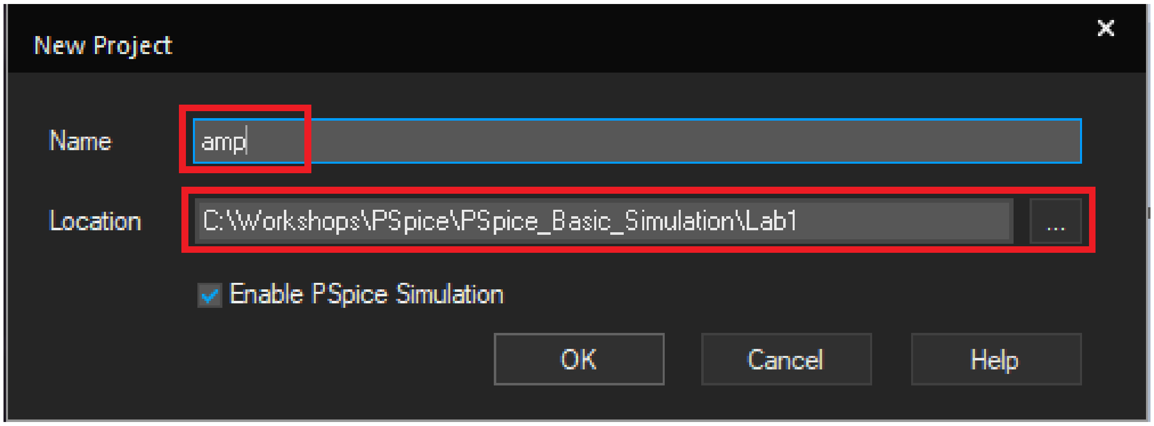


Figure 1-3: Naming the project and setting the location

The module1 folder will contain the files that make up the new project. It has been seeded with a couple of files to make the workshop go smooth, including a transistor PSpice model file, which you will use shortly.

4. In the **Create PSpice Project** window, select **Create based upon an existing project**.

5. Use the pull-down menu to select the **empty_all_libs.opj** entry to have access to all PSpice libraries supplied by Cadence. Click **OK**.

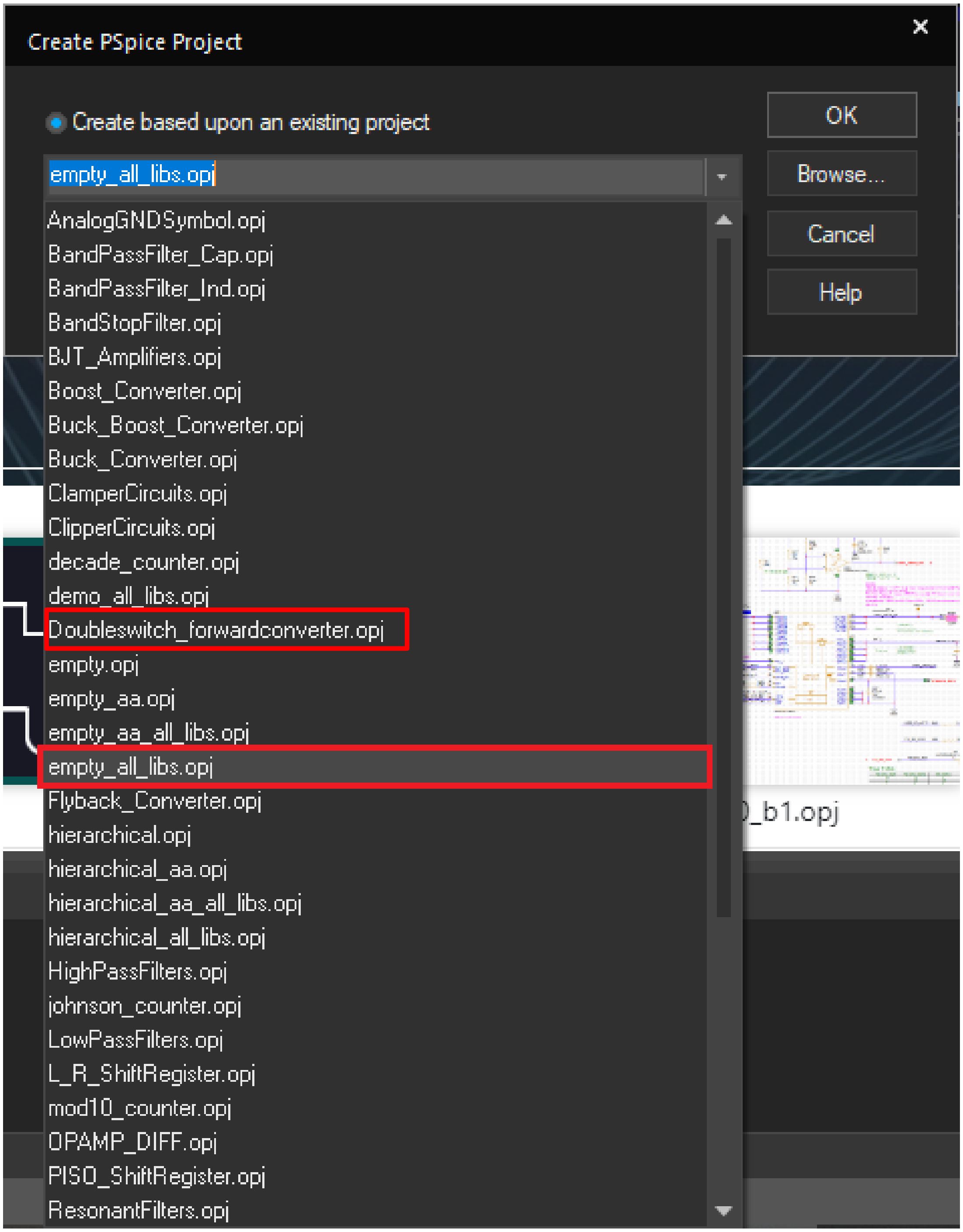


Figure 1-4: Create PSpice project with access to all libraries

Capture will now open the amp project and you will see the Project Manager.

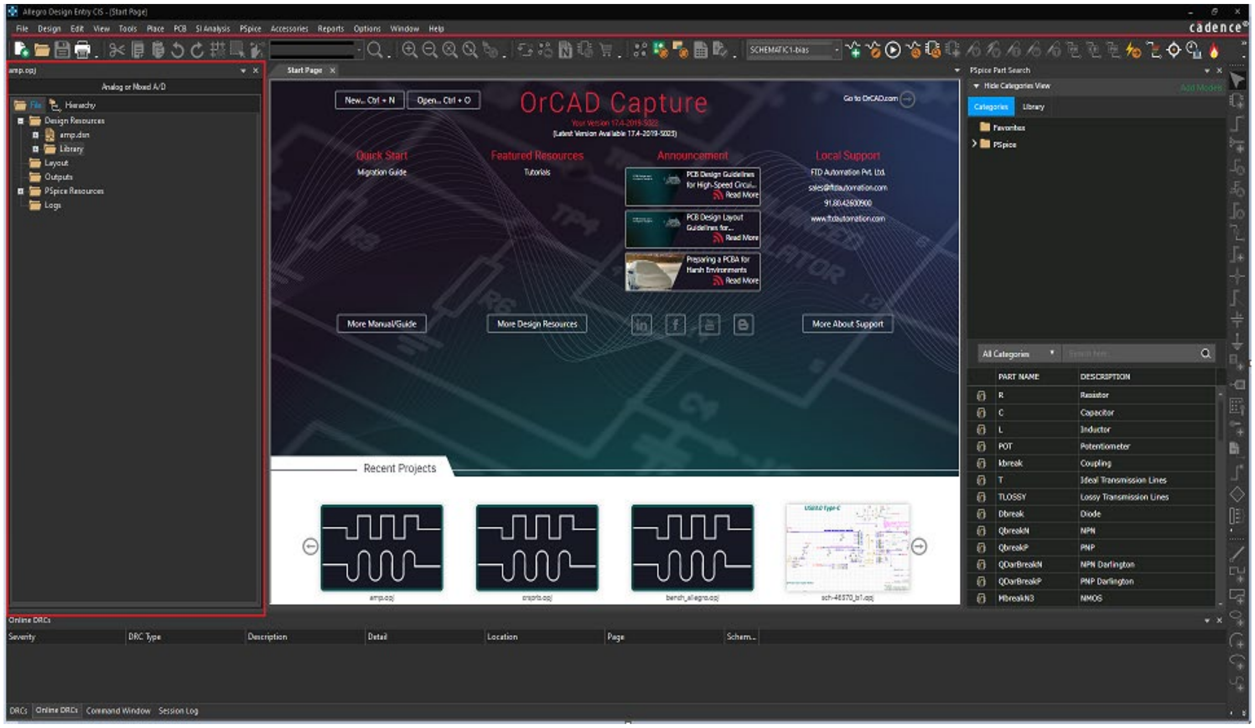


Figure 1-5: Project Manager

Expand the design by clicking **+** in front of the **amp.dsn** icon to list the design pages.

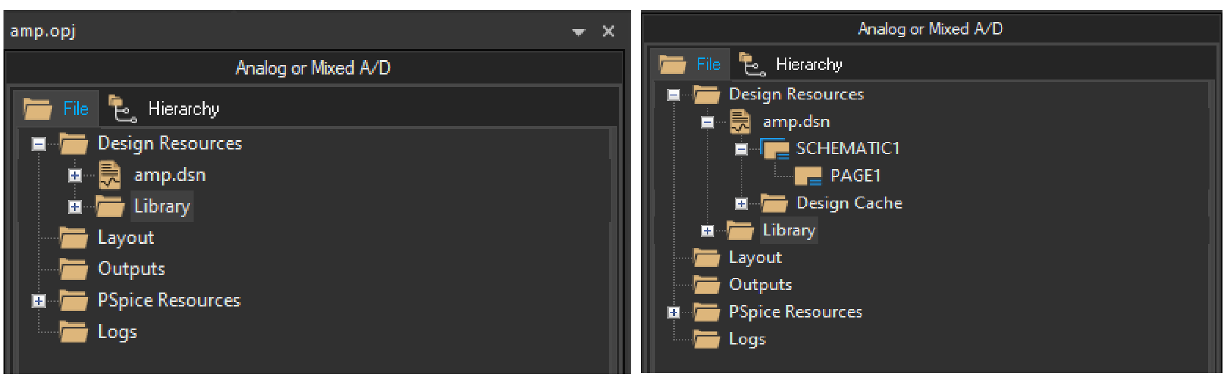


Figure 1-6: Before **After**

6. Double-click on **PAGE1** to open the schematic editor.

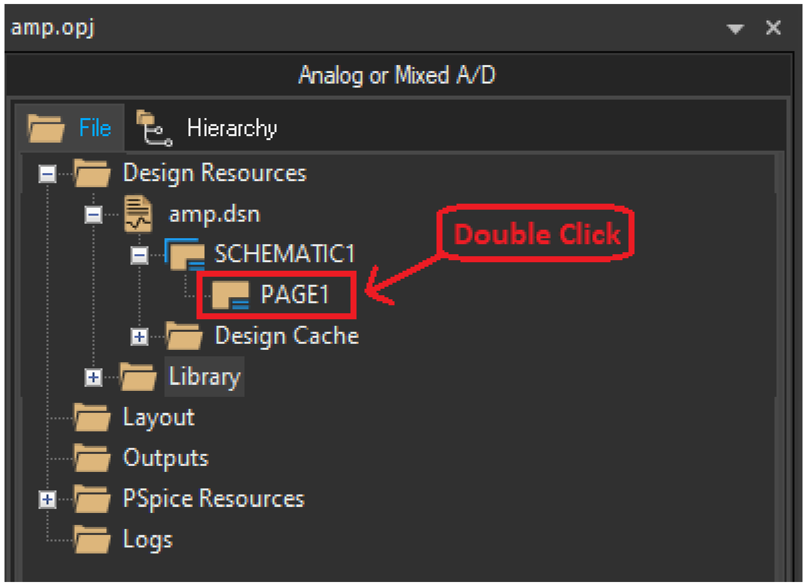


Figure 1-7: Opening the schematic editor

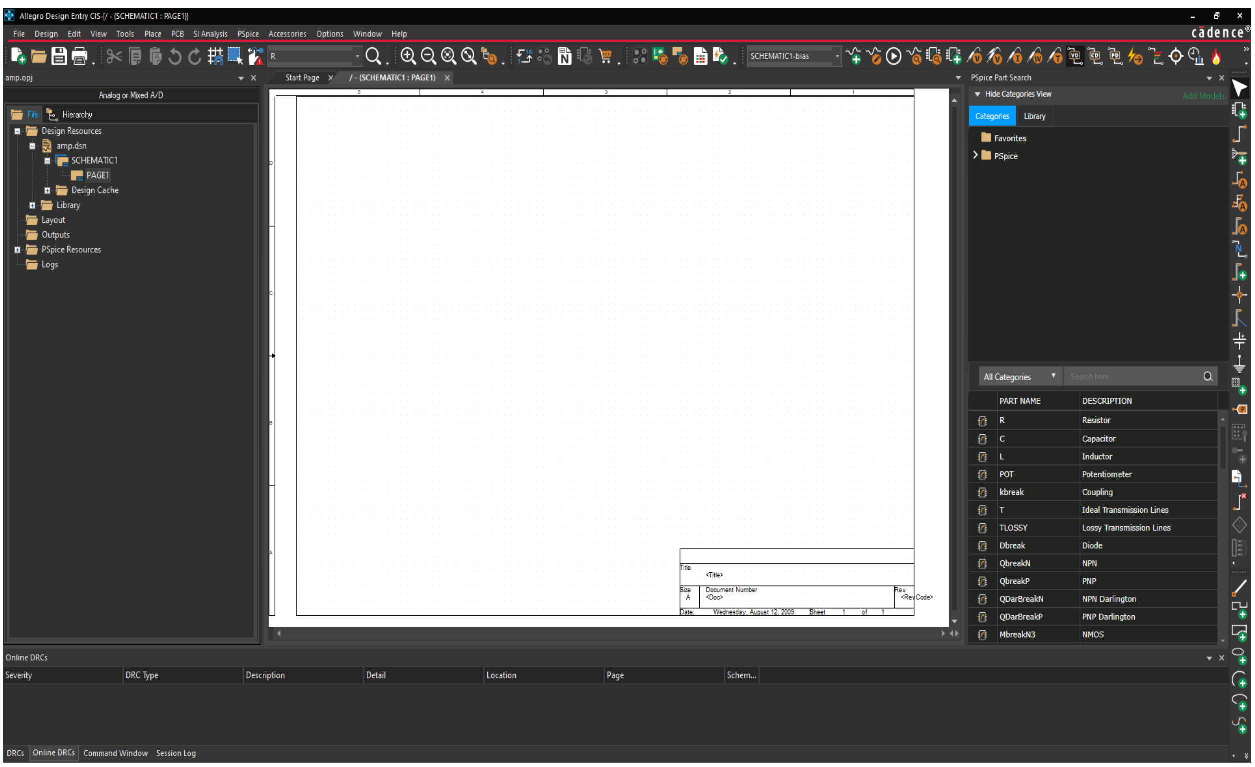


Figure 1-8: Capture schematic page

Leave Capture open. Now, you will import a transistor PSpice model that was downloaded from a vendor’s website.

Lab 2: Importing a Vendor PSpice Model

7. Start the PSpice Model Editor by selecting **All Programs > Cadence Release SPB 17.2-2016 > Model Editor or Cadence PCB Utilities 17.4-2019 > PSpice Model Editor 17.4**.

8. If prompted, select **PSpice Simulator** as the product and check the “Use as default” option. Now, click **OK**. The PSpice Model Editor opens.

   If prompted as “Select Design Authoring Tool” when the Model Editor starts, select **Capture** and check “Don’t ask me again”.

9. Select **File > New**.

10. In the Model Editor window, start the Model Import Wizard by selecting **File > Model Import Wizard**. The Model Import Wizard opens, as shown in Figure 1-9.

11. In the **Enter Input Model Library** field, browse to the **C:\Workshops\PSpice\PSpice_Basic_Simulation\Lab1** folder and select the file **new_npn.lib**. Select **Open** to complete the action.

    The **Destination Library** field is auto-populated with the correct path. This is where the library/symbol (to be created during the import) will be saved.

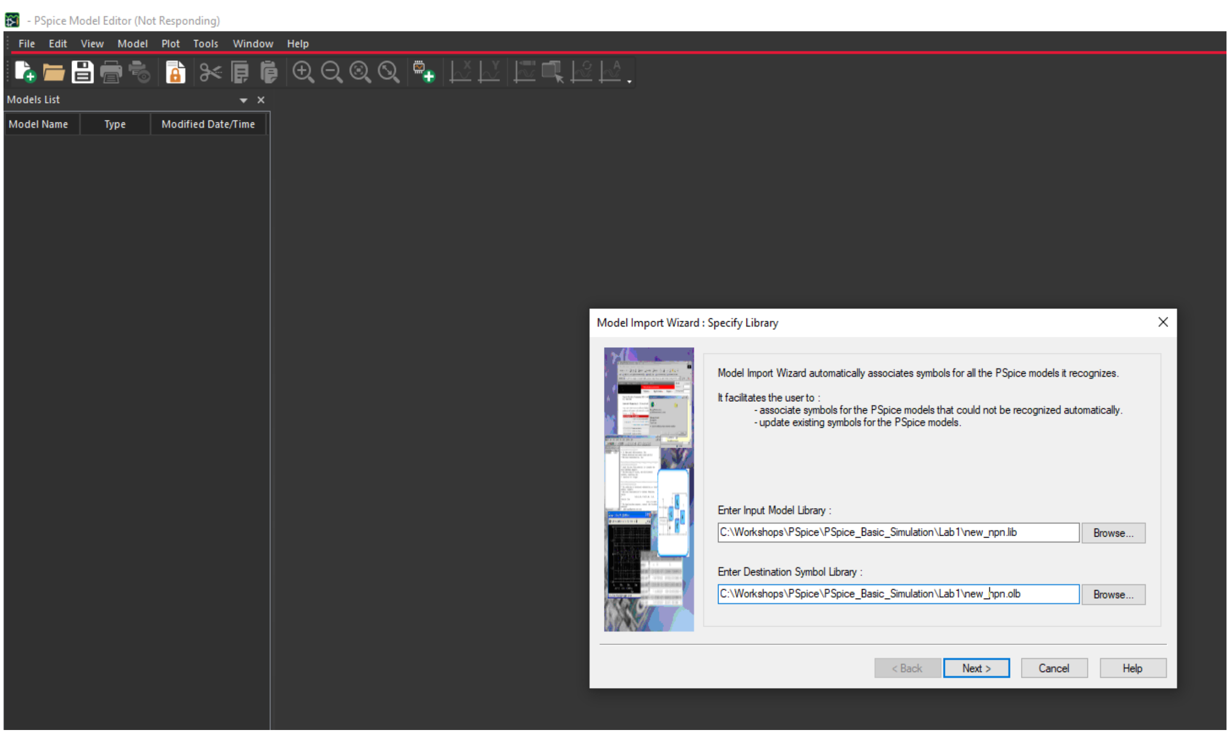


Figure 1-9: PSpice Model Editor and Model Import Wizard

12. Select **Next** to begin the import process.

    You are now presented with the **Associate/Replace Symbol** form, as shown in Figure 1-10. Note that a matching symbol is automatically assigned to the new model and you also have the option of replacing that symbol with others of the same terminal count. There are similar symbol templates for more than 50 different model types, including op amps, magnetic parts, SCRs, and so on. These symbols can be customized to match your corporate library.

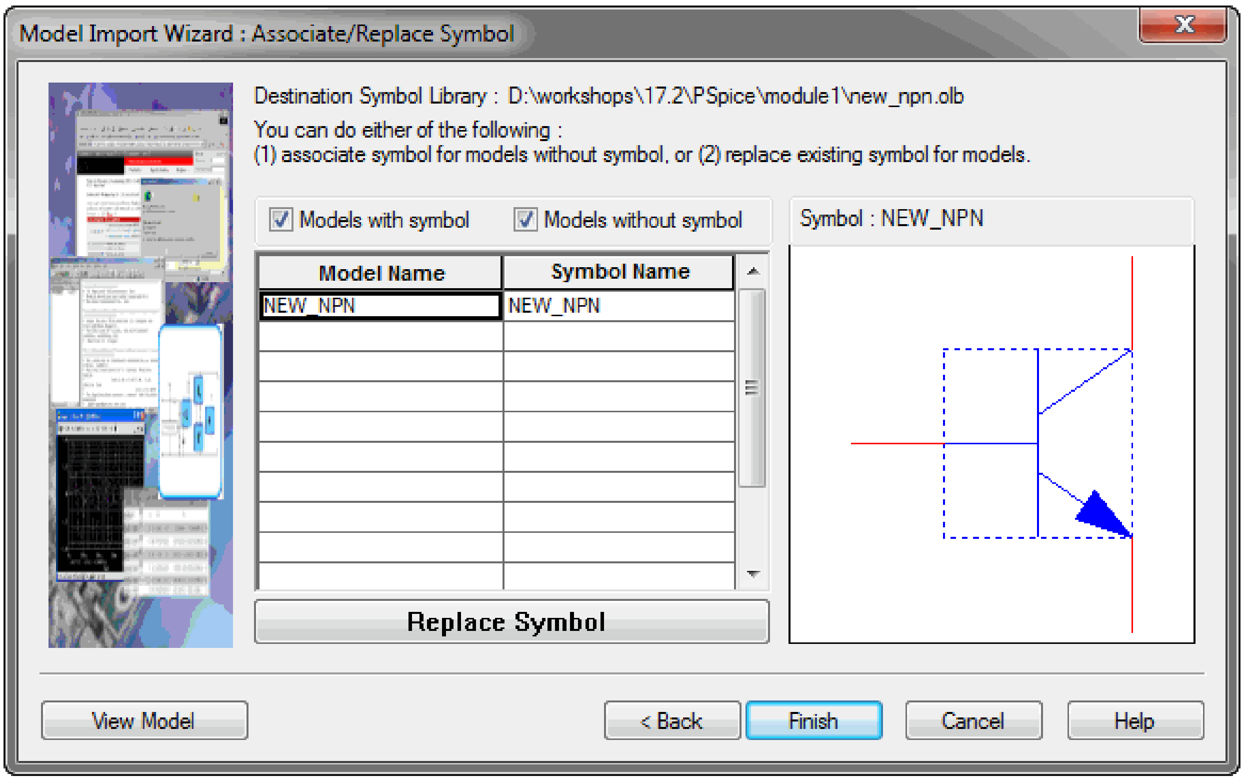


Figure 1-10: Symbol Association

13. You can select **View Model** to see the model, and then click **OK**.

14. Select **Finish**, which will bring up the import log. Now, click **OK** to complete the model import process.

15. Close (**File > Exit**) the Model Editor.

A library and a symbol have been created for the vendor model and placed into the project folder (**PSpice\module1**). You will now select the library so that you can instantiate the transistor onto the schematic.

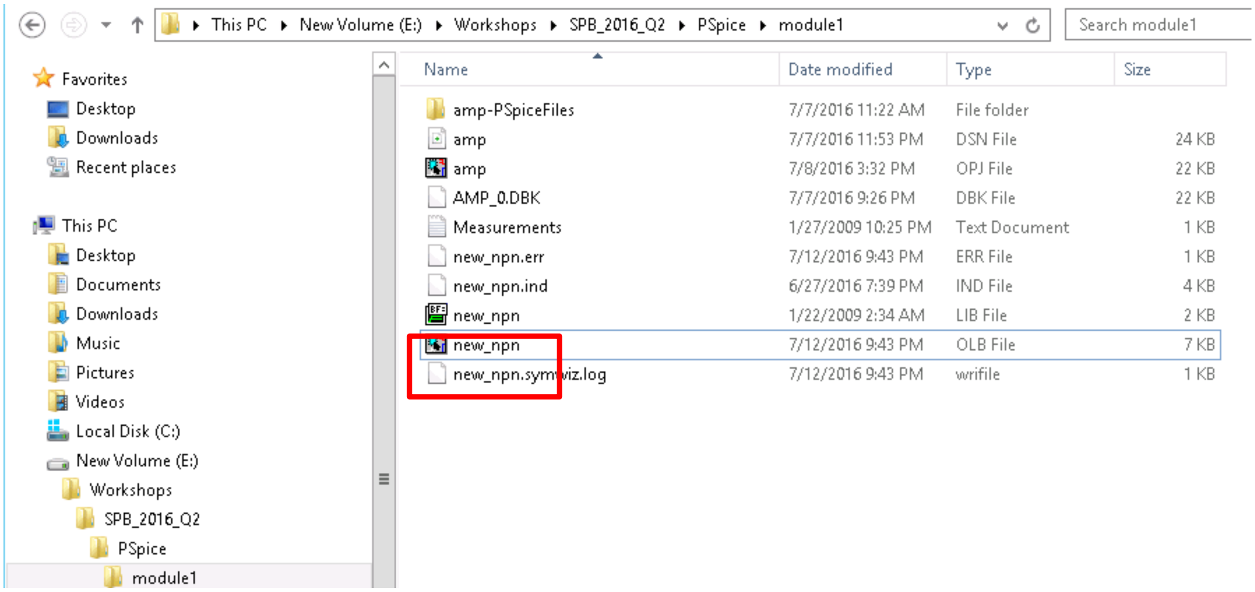


Figure 1-11: Library and Symbol Files

16. Return to Capture and select the **Place Part** icon on the right-hand side or select **Place > Part** in the Capture menu. This will add the Place Part GUI to the Capture canvas.

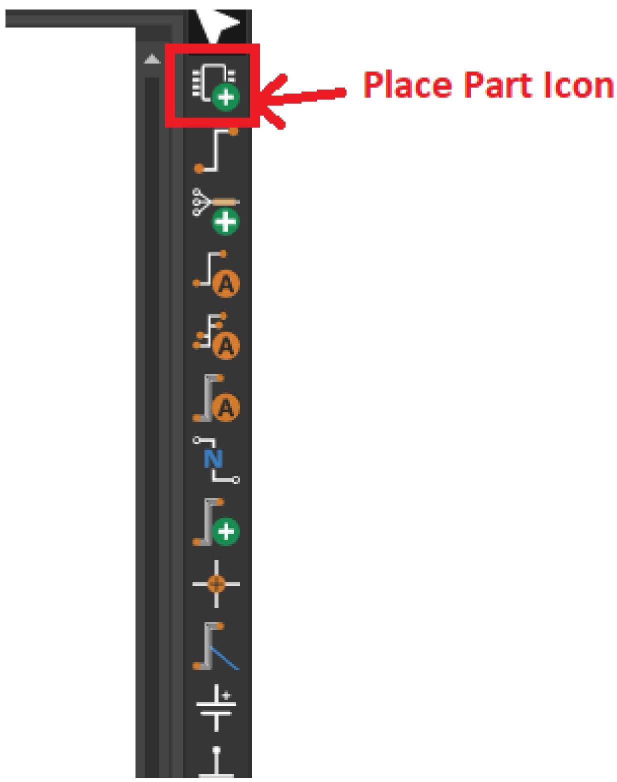


Figure 1-12: Place Component icon

17. Select the **Add Library** icon.

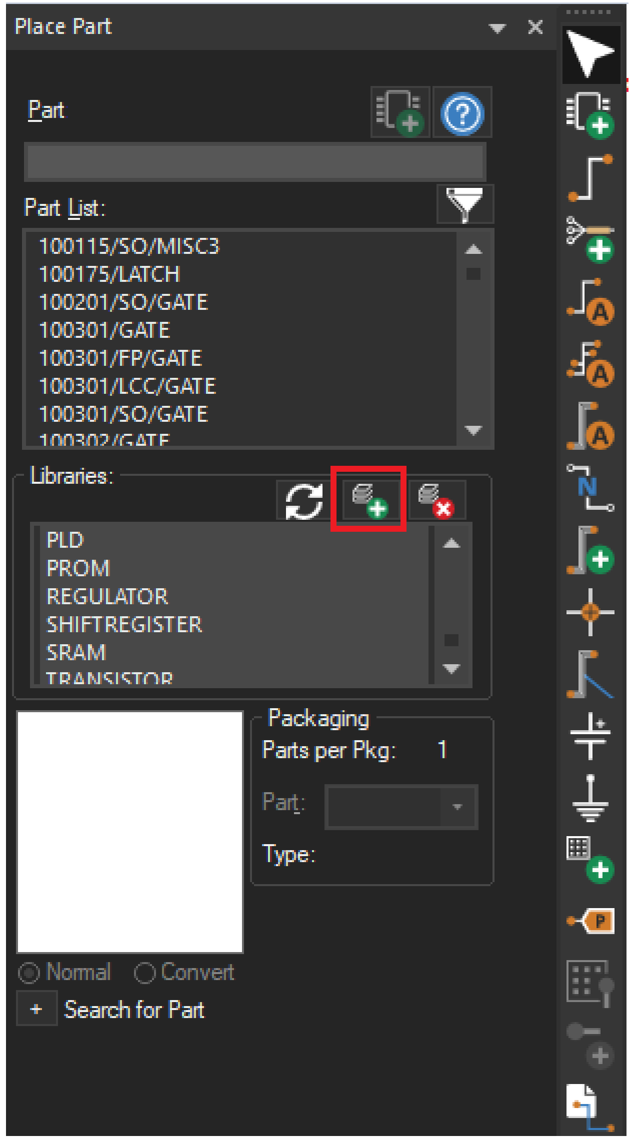


Figure 1-13: Add Library icon

18. Browse to the **module1** folder and select the **new_npn.olb** file. Select **Open** to complete the action.

19. The library and its contents are now available for adding. Click on **NEW_NPN** in the **Part List** pane. Note the symbol preview for the NEW_NPN part.

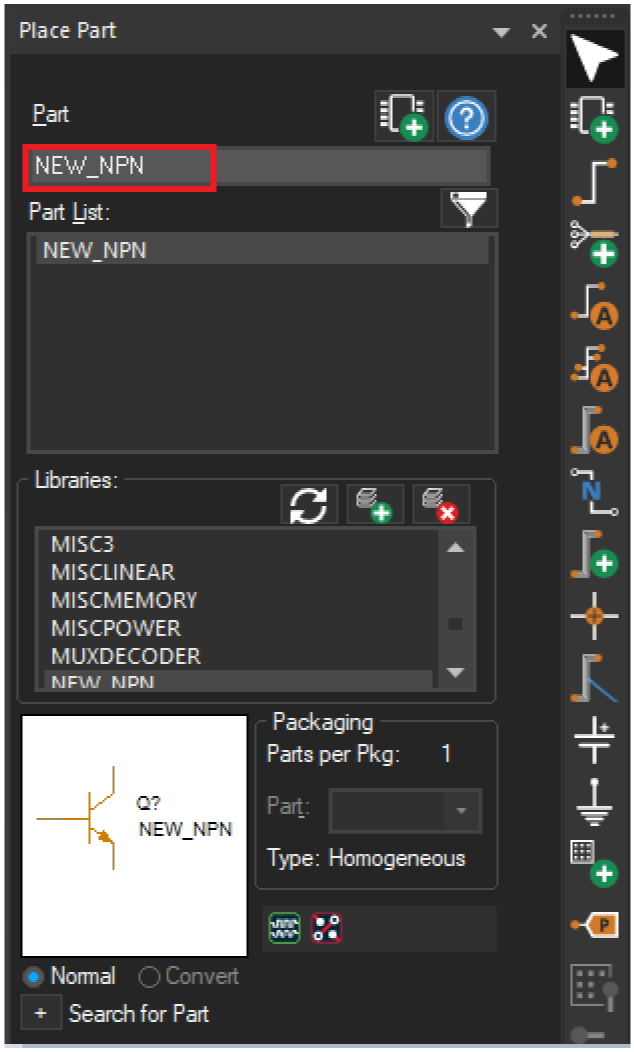
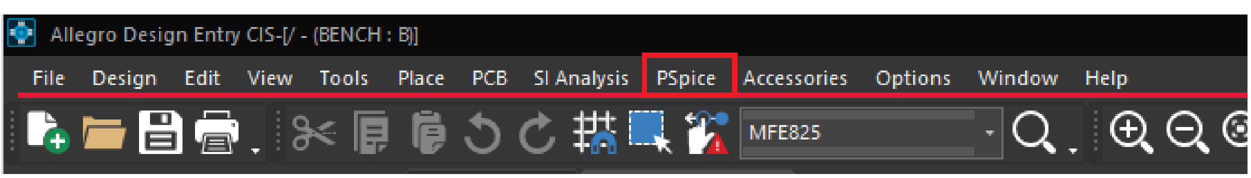


Figure 1-14: NEW_NPN now available for placement

PSpice Integration in OrCAD Capture

OrCAD Capture provides fast, easy, and intuitive design entry, along with highly integrated flows supporting the engineering process. OrCAD Capture does not require you to configure the schematic capture environment for analog design. Once the design is created as an analog design, the environment is set up for you to immediately start design entry. All PSpice-specific toolbars are available.



The PSpice toolbar allows to create a simulation profile, run the simulation, and place probes.

Figure 1-15: PSpice Capture toolbar

Lab 3a: Schematic Entry – Placing Components

Figure 1-16 shows an image of a common-emitter amplifier that you will create for the first exercise. You will later move on to a two-transistor RF amplifier and then to a band-pass filter to explore some of the advanced capabilities of the PSpice simulator.

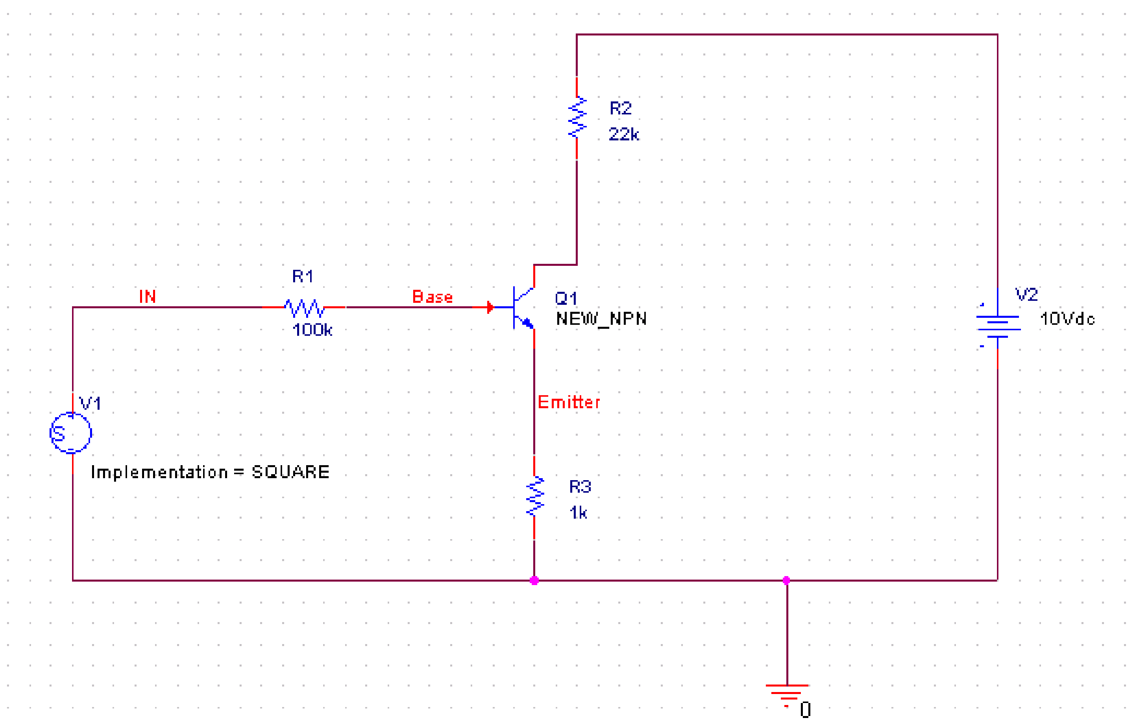


Figure 1-16: Common-Emitter Amplifier schematic in OrCAD Capture

For the majority of this design (standard parts), you will use Place Part to add the required components. You will also add net aliases and the ground component.

Use the Place Parts GUI to add components. If you are not sure which library the component resides in, highlight the library or libraries and start entering the part name in the name field. Double-click on the component and you can then place the part on the canvas.

You should still have NEW_NPN open from Lab 1; if so, skip to step 22.

20. Select the **Add Component** icon along the upper-right edge of Capture. The **Place Part** window appears.
21. Select only the **NEW_NPN** library and then highlight the **NEW_NPN** cell, as shown in Figure 1-17

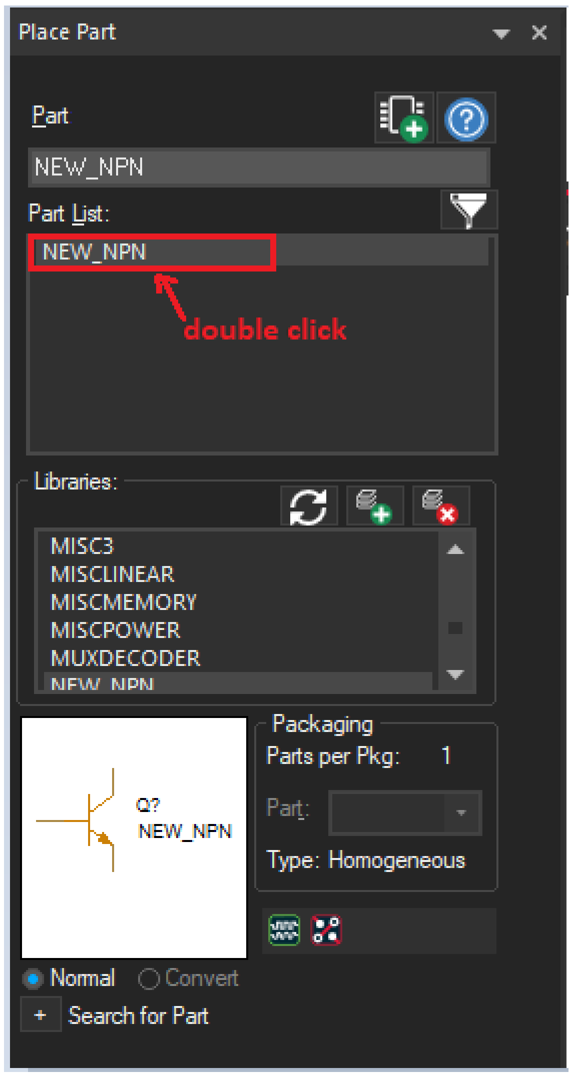


Figure 1-17: Place Part GUI

22. Double-click on the name **NEW_NPN** and the component will appear on the cursor in the schematic canvas. Place the part in the center of the canvas. Right-click on **End Mode** (or press the **Esc** key) to conclude placement of a component.

23. Add the remaining components (except for the ground symbol) to create the design. Figure 1-18 shows the components required to create the design and the libraries that they reside in.

Part Type	Part Name	Library Name
Stimulus	VSTIM	sourcestm
Voltage Source	VDC	source
Resistor	R	Analog
NPN	NEW_NPN	NEW_NPN

Figure 1-18: Table of Parts

24. Right-click **End Mode** (or press the **Esc** key) to conclude the placement of a component. If you happen to place too many parts, you can use Undo (Ctrl+z) to remove it. During the placement, you can use the right mouse button to rotate a part.

25. Performing right-click on **End Mode** OR using the **Esc** key in the previous step takes Capture out of the “Add” mode. If this had not been done, an additional left-click on the canvas would have attached a second instance of the component to your mouse, allowing you to place it by left-clicking at the desired location.

26. Once the components have been placed, wire the components as shown in Figure 1-16. Wires will bend as you move them from point to point. Start by right-clicking on a pin and then move to another component’s pin to create the connection. To add a wire, enter the wiring mode by selecting **Place > Wire** or typing in **W**. While right angles are automatic during the wiring, you can do a left click to force a right-angle location. To leave a wire in space, double-click or right-click and select **End Wire**.

27. PSpice requires a special ground symbol that sets the net with a node=0 value. All SPICE simulators require a DC path to ground, and this is the method that PSpice uses to satisfy the SPICE requirement. To add the ground symbol, select **Place > Ground**.

28. To change component values on the schematic canvas, double-click on the property and change its value.

    Change the component values so that they are the same as shown in Figure 1-16. When names get long or the page is crowded, you can drag the properties to locations that are more suitable. In this example, you should move the 10Vdc property to a better location.

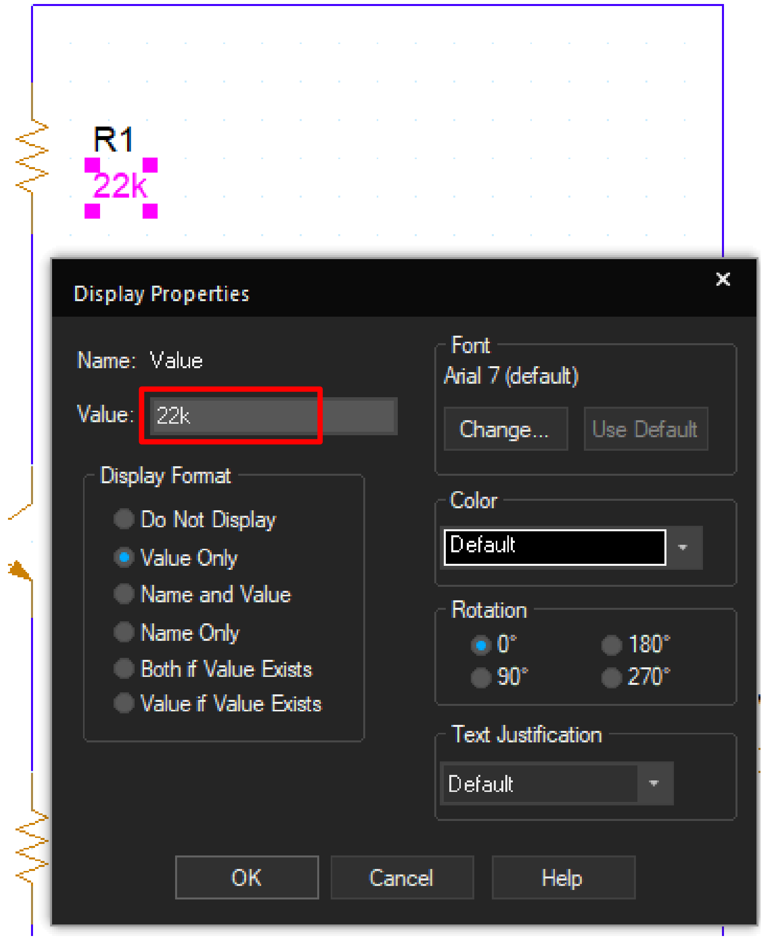


Figure 1-19: Display Properties form

29. To put a name on a net, you can select the net you want to attach the signal to.

    Add the **IN**, **BASE**, and **EMMITER** signals, as shown in Figure 1-16. Select **Place > Net Alias** to add the signal names.

30. Change the value of the **Implementation** property on the voltage source to **SQUARE**.

    In Module 2, you will create a waveform using the Stimulus Editor and attach the waveform SQUARE to the source.

31. Once you have completed the design, select the **Zoom All** icon to see the entire design.

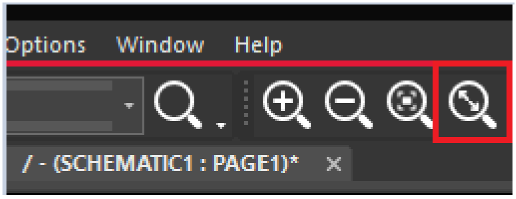


Figure 1-20

32. Save the design.

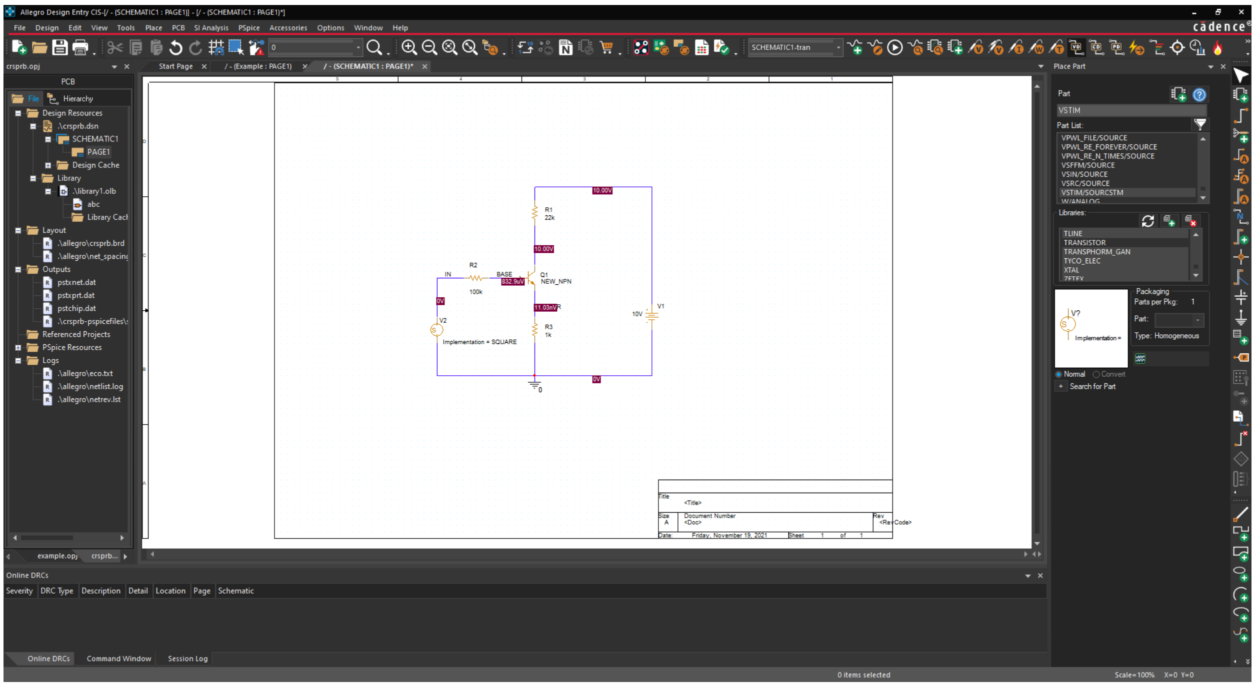


Figure 1-21: Completed design

Lab 3b: Creating and Viewing the Netlist

Note: Manually creating a netlist is not a prerequisite to simulate the design – the netlist is created automatically (if necessary) when a simulation is initiated. This step will help validate the design netlist and is a good checking point.

33. Select **PSpice > Create Netlist** (save, if prompted). The netlist is created using the Reference Designators that appear on the components. Capture automatically adds Reference Designators when a component is placed. You may change these values.

34. Select **PSpice > View Netlist**. The netlist is displayed, as shown in Figure 1-21 (it may not match exactly).

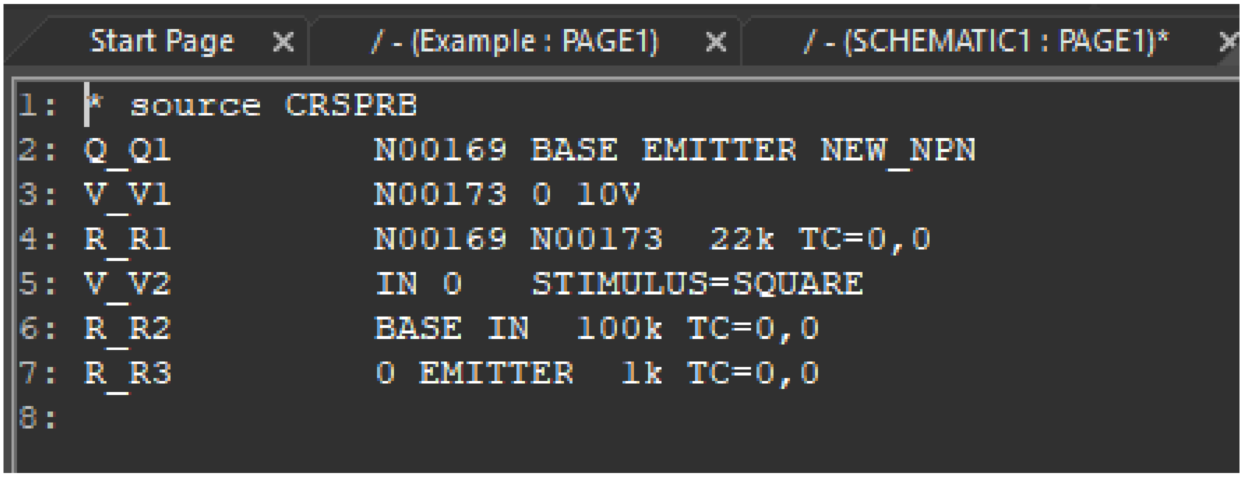


Figure 1-22: Netlist for the example design

35. Close the netlist viewer by right-clicking on the netlist tab and selecting **Close**.

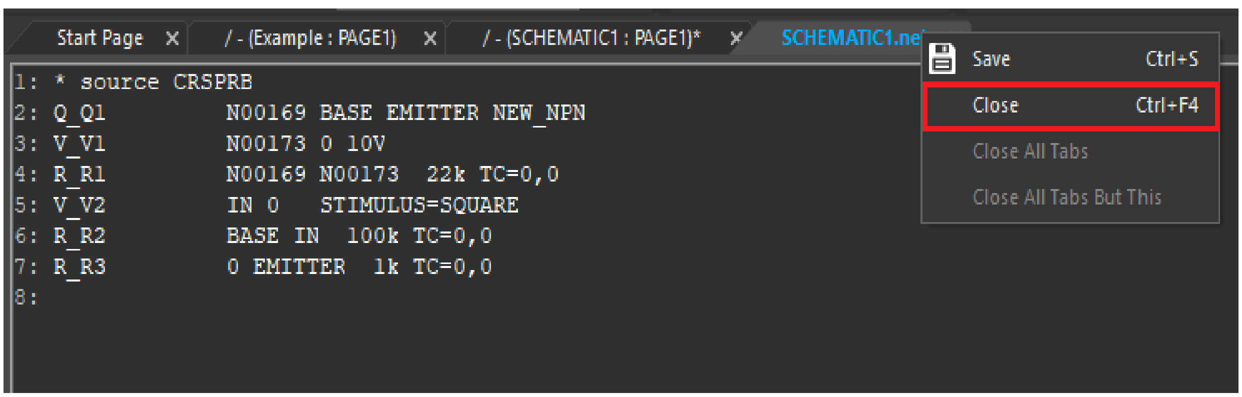


Figure 1-23: Closing the netlist view

You may clean up the schematic by moving/rotating the text. An image of the completed design is given below. Reference designators for the three resistors may not match your design but that will not impact the results.

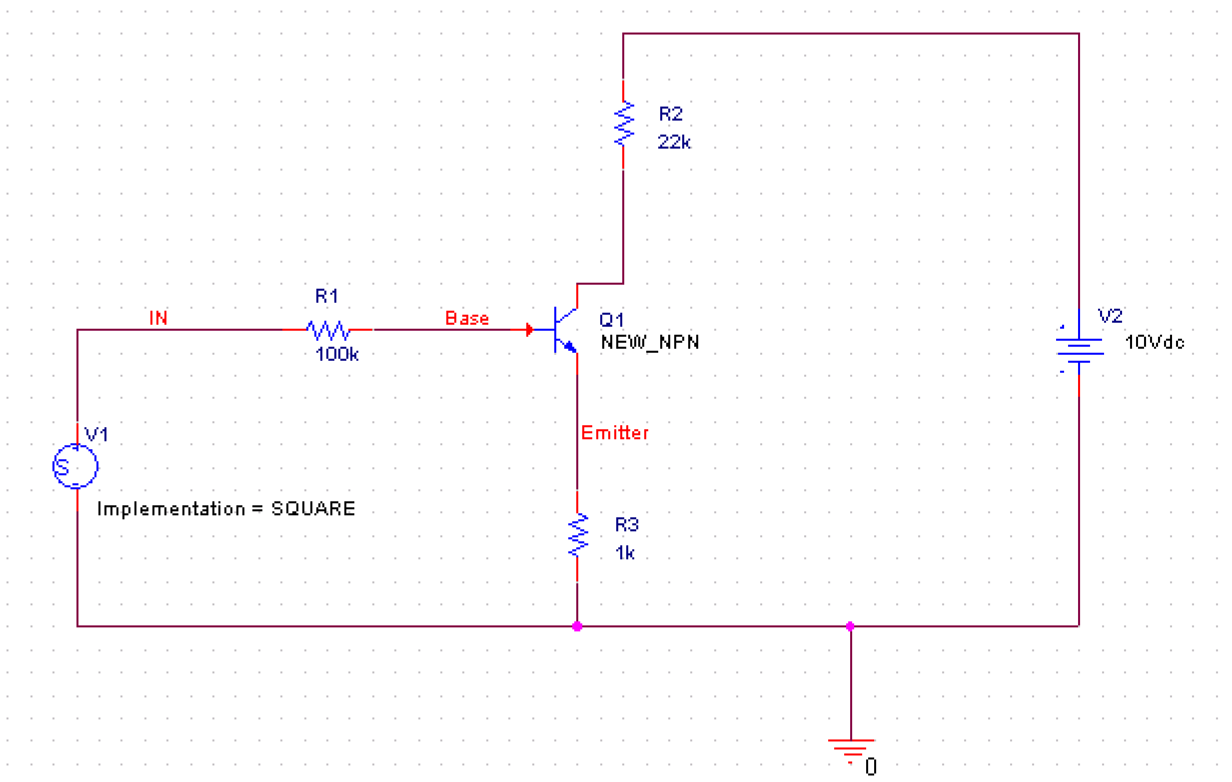


Figure 1-24: Completed schematic diagram

This completes Module 1 of this workshop. **Leave all tools open**.

Module 2: PSpice Simulator Basics

This module covers:

- Simulation Setup
- Basic Simulation
- Viewing Simulation Results
- Checkpoint/Restart
- Assertions
- Measurement Expressions

Loading the Completed Schematic

If you feel that you may not have completed the design from Module 1 entirely, you may wish to follow the steps given below to load a completed version of it for use in this module.

a. Exit Capture (**File > Exit**) to close the current design. You may save if you wish, but you might encounter errors if the design is not correct.

b. In Capture, select **File > Open Design**, navigate to **module2\amp.dsn**, and select **Open**.

Note: Because of the option of continuing with your Module 1 design or loading the completed design for Module 2, there may be a mismatch in some displayed paths. The remaining text of this module will assume that the completed design in the module2 folder is opened as per the above instructions. If you are continuing this module with your Module 1 design, you must understand that any references to the module2 folder should be substituted with the equivalent module1 path.

Lab 4: Creating a Simulation Profile

You will now create and configure a simulation profile for a simple 300us time-domain simulation. There is no limit to the number of simulation profiles that can be defined in a project.

1. Select **PSpice > New Simulation Profile**.

2. In the **New Simulation** form, enter **td300** (to signify 300us, time-domain) into the **Name** field and click on **Create**.

   Note: If prompted for a choice of products, choose PSpice Simulator and check ‘Use as default’.

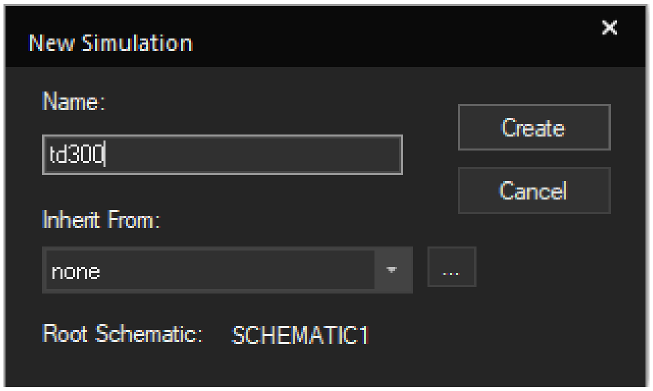


Figure 2-1: New Simulation Profile form

The **Simulation Settings** form is presented. In the **Analysis** tab, select **Time Domain (Transient)** for **Analysis Type** and set **Run To Time** to 300us, as shown in Figure 2-3.

Note: The **Simulation Profile Editor** might launch behind **Capture** in 17.2; so, you can go to the taskbar and select Simulation Profile Editor to bring it forward.

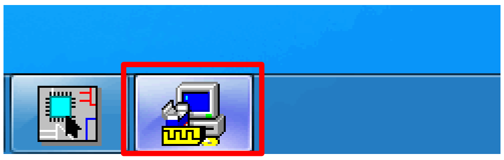


Figure 2-2: Simulation Profile Editor

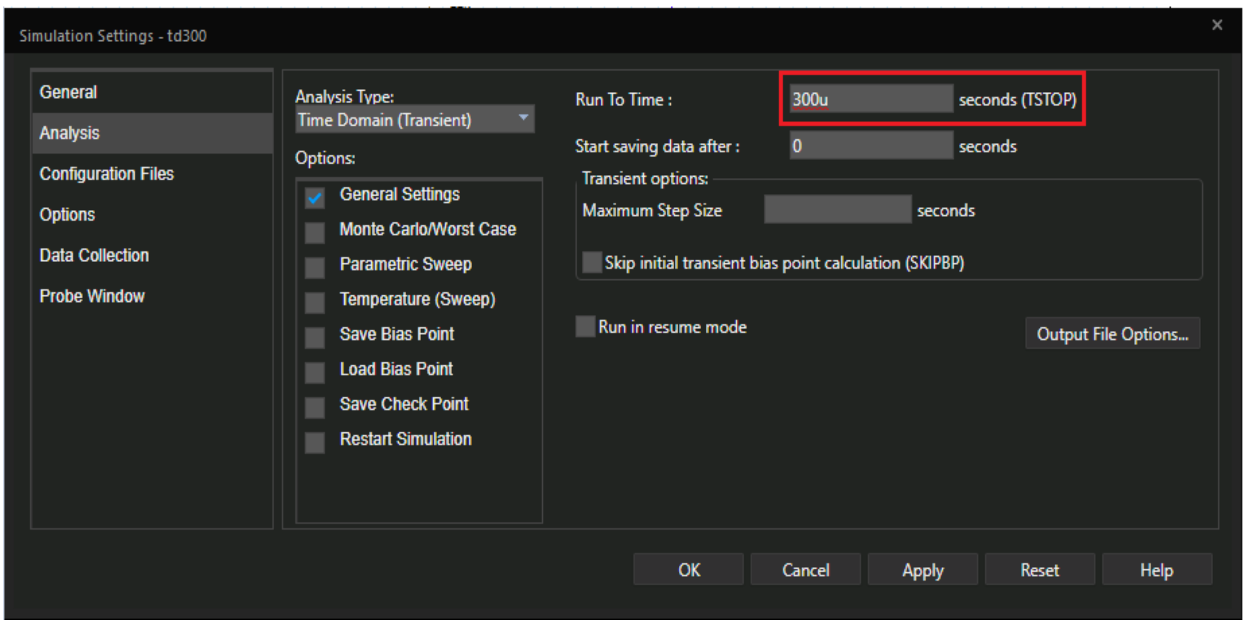


Figure 2-3: General settings for Time-Domain Analysis

3. In the same tab, check the **Save Check Point** checkbox and set **Simulation Interval** to **100us**, as shown in Figure 2-4.

   This will cause the simulation state information to be saved at 100us (simulation time) intervals as part of the Checkpoint/Restart feature. You can later start a simulation (with any desired simulation settings) from any of these checkpoints. This can save your time by avoiding needless re-simulations of a design's stabilization time, for instance.

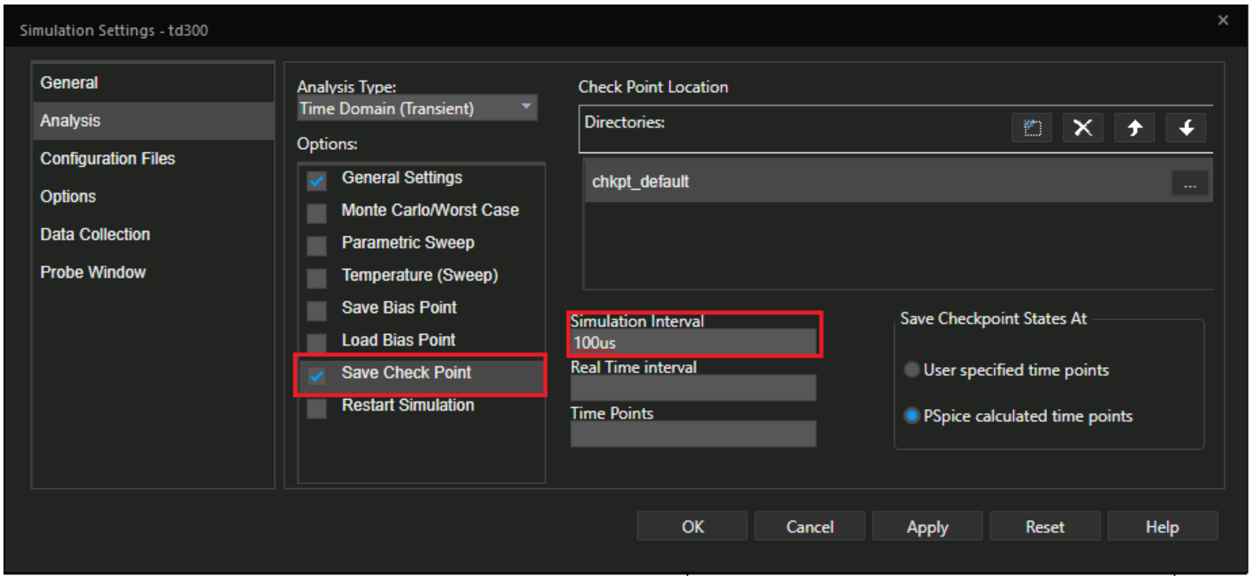


Figure 2-4: Check Point Settings

In Module 1, you generated (using new_npn.lib as an input file to the Model Import Wizard) and placed an NPN transistor. Although the schematic symbol is now part of the project, the model itself has not been made available to the simulator. This is taken care of via the Configuration Files tab of the simulation profile editor.

4. In the **Configuration Files** tab, select **Library**.

5. Select the **Browse** button next to the **Filename:** field (see Figure 2-5). Browse and select the vendor library file found in **module2\new_npn.lib**. After selecting **new_npn.lib**, select **Open** in the file browser.

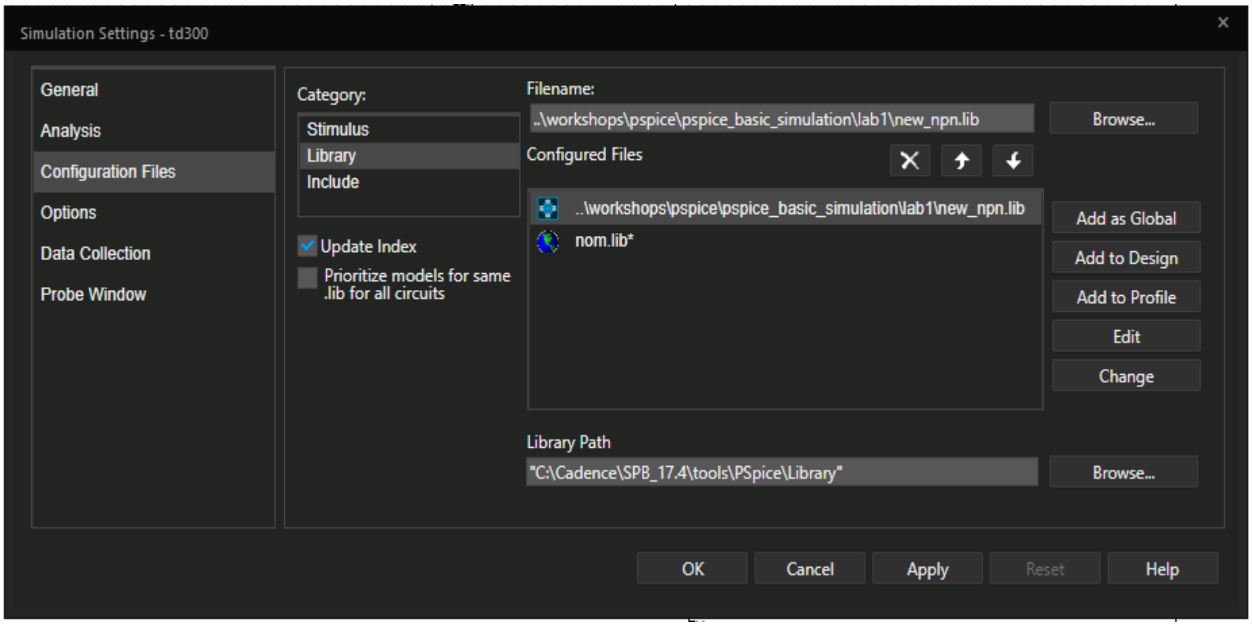


Figure 2-5: Including new_npn.lib

Libraries can be linked at the global (computer), design, or simulation profile level. Each level has its corresponding scope of accessibility. You will add this library to the design, which means that any simulation profile in this project will have access to the library, and thus, any models contained therein.

6. Select **Add to Design** to complete the action. The form should now resemble Figure 2-6.

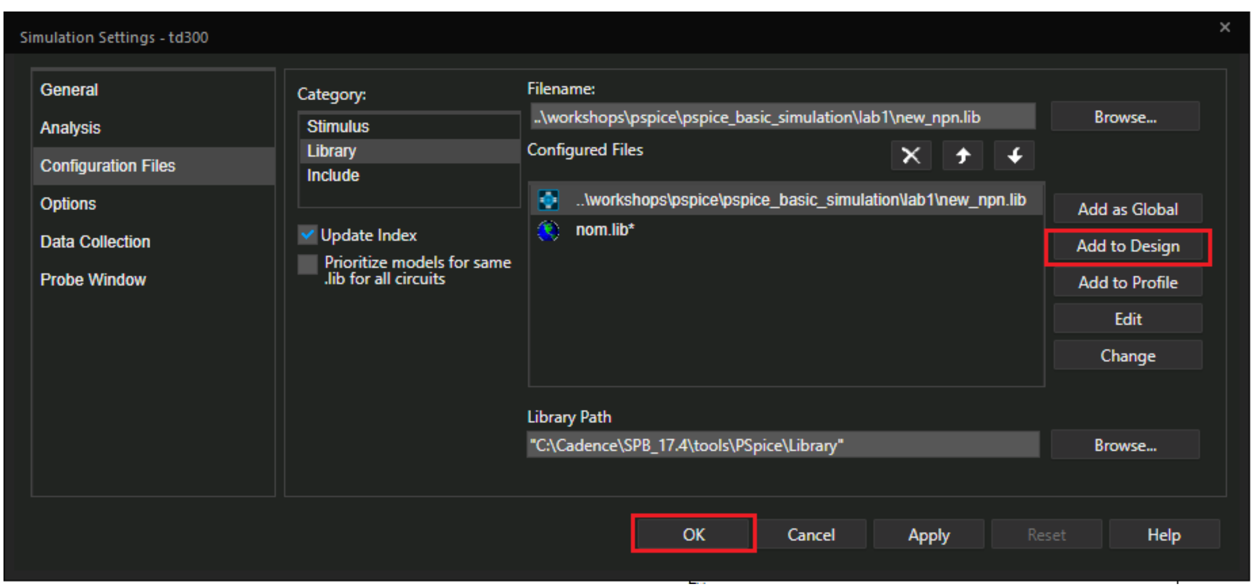


Figure 2-6: Add new_npn to simulation library

The AutoConverge feature allows PSpice to simulate more reliably by relaxing certain tolerances and automatically resuming simulation with the new settings, should a convergence problem arise. This is especially useful when simulating power electronics designs, where discontinuous behavior is not uncommon.

7. In the **Options** tab, select **AutoConverge** under **Analog Simulation** and enable the **AutoConverge** option, as shown in Figure 2-7. Click **OK** on the **AutoConverge Options** form.

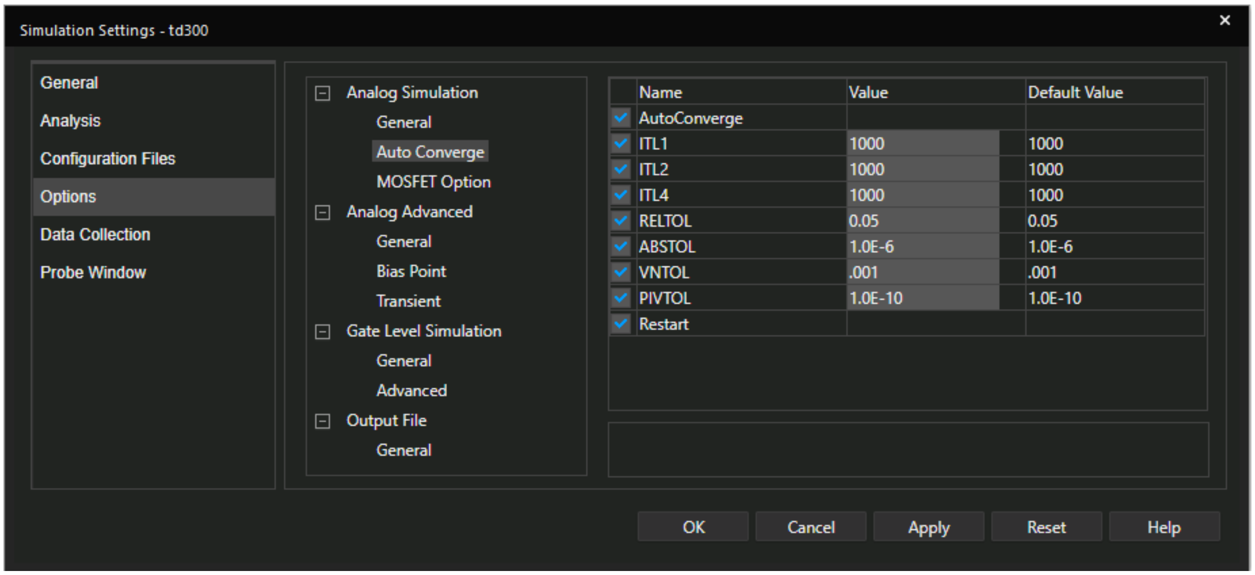


Figure 2-7: AutoConverge Settings

8. Set the number of **THREADS** to **2**. PSpice supports multiple processor threads based on the number of processors in the system. Setting the value to 0 will allow PSpice to use all available processors.

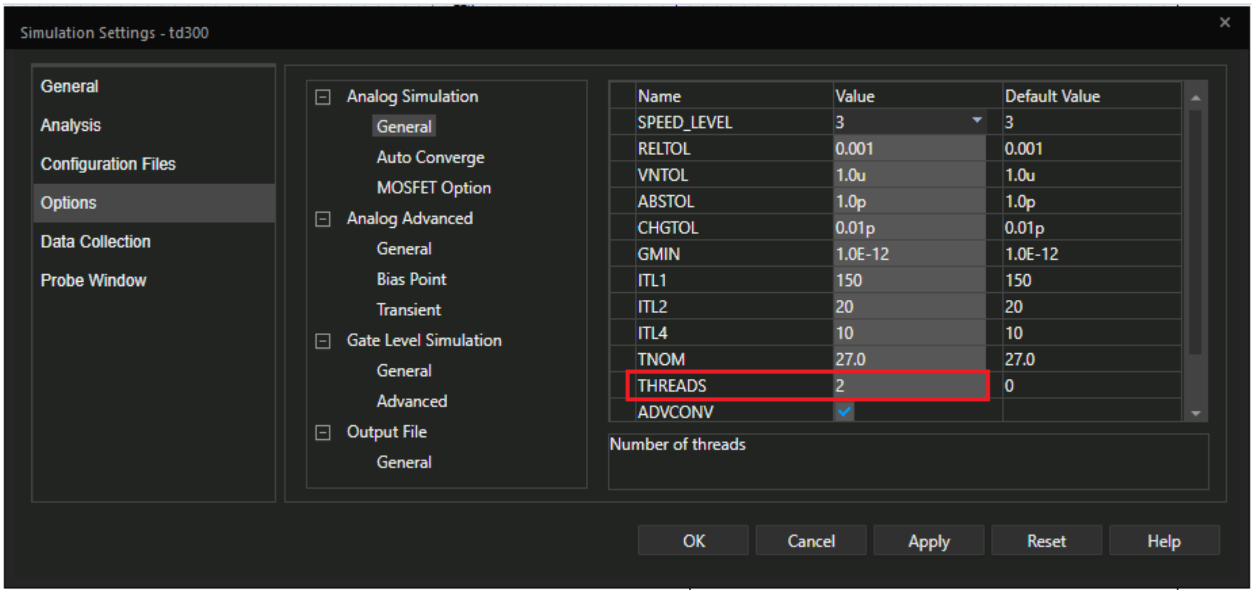


Figure 2-8: Setting threads

9. Go to **General**, **Bias Point**, and **Transient** options under **Analog Advanced** to visualize robust options available to the simulator. Descriptions of these options are given in the PSpice user guide. Press **Cancel** to dismiss the window.

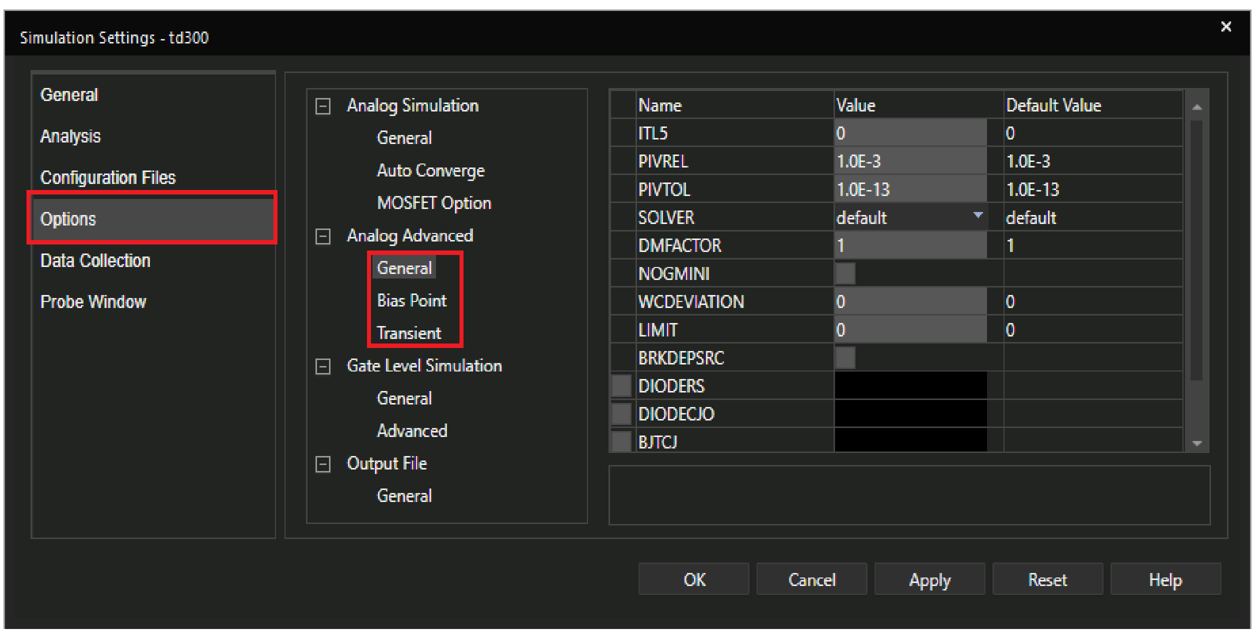


Figure 2-9: Advanced Analysis Options

10. In the **Probe Window** tab, adjust settings as shown in Figure 2-10.

The **All markers on open schematics.** option directs PSpice to automatically produce a trace (waveform) for each probe symbol placed on the schematic. The traces will share a common X- and Y-axis. You will use the **Last Plot** option later in this Module.

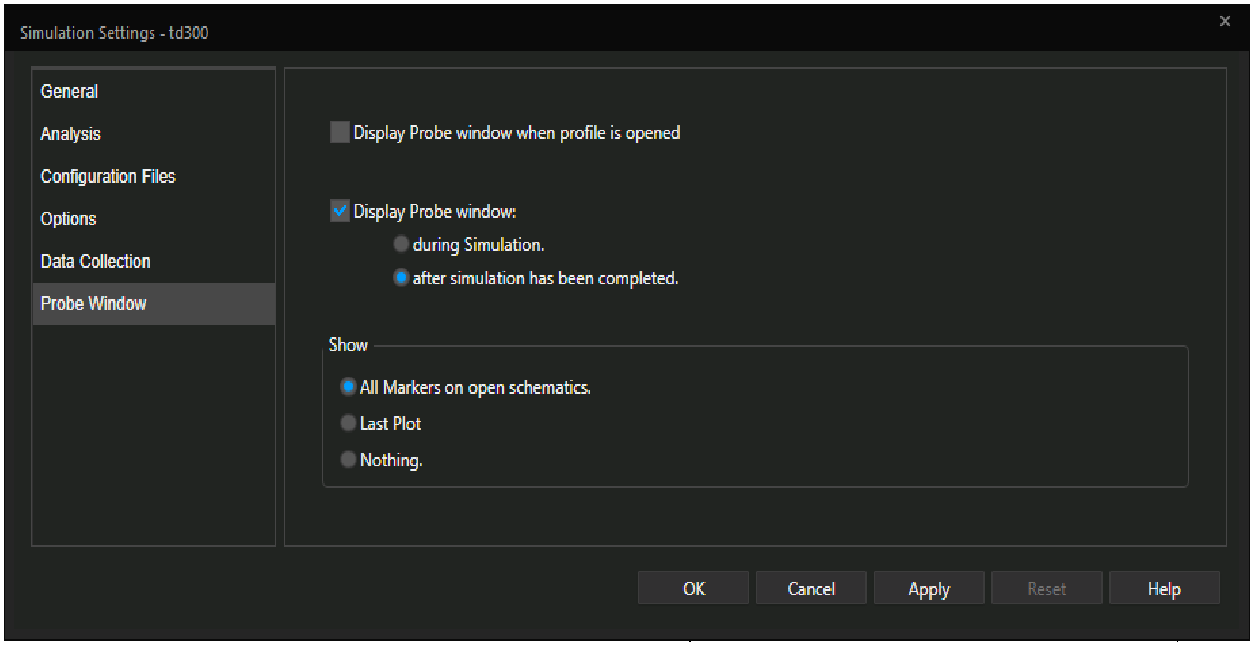


Figure 2-10: Probe Settings in the "td300" Simulation Profile

11. Select **OK** on the **Simulation Settings** form and select **Yes** to allow the creation of the new checkpoint directory.

    The simulation profile setup is complete. Note that now, the analog toolbar shows the **td300** simulation profile (the only existing simulation profile in this project) as the current profile. Actions requiring a simulation profile (simulating, defining stimuli) will use td300 since it is selected here.

Figure 2-11: Analog Toolbar showing new Simulation Profile

Lab 5: Creating the Stimulus

A stimulus generator is present in the design that identifies a stimulus called SQUARE. This stimulus has not yet been defined. You will do this now.

12. Click to select on the stimulus symbol (labeled "S" in the schematic) and right-click to select **Edit Stimulus**.

13. The **Stimulus Editor** appears.

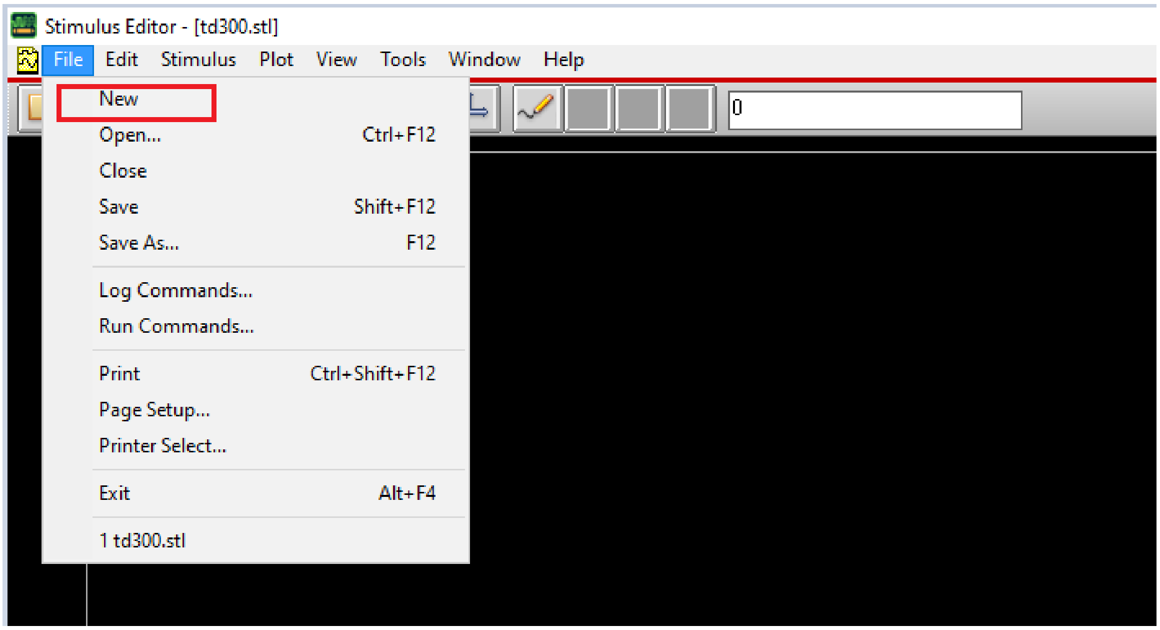


Figure 2-12: Creating a new Stimulus

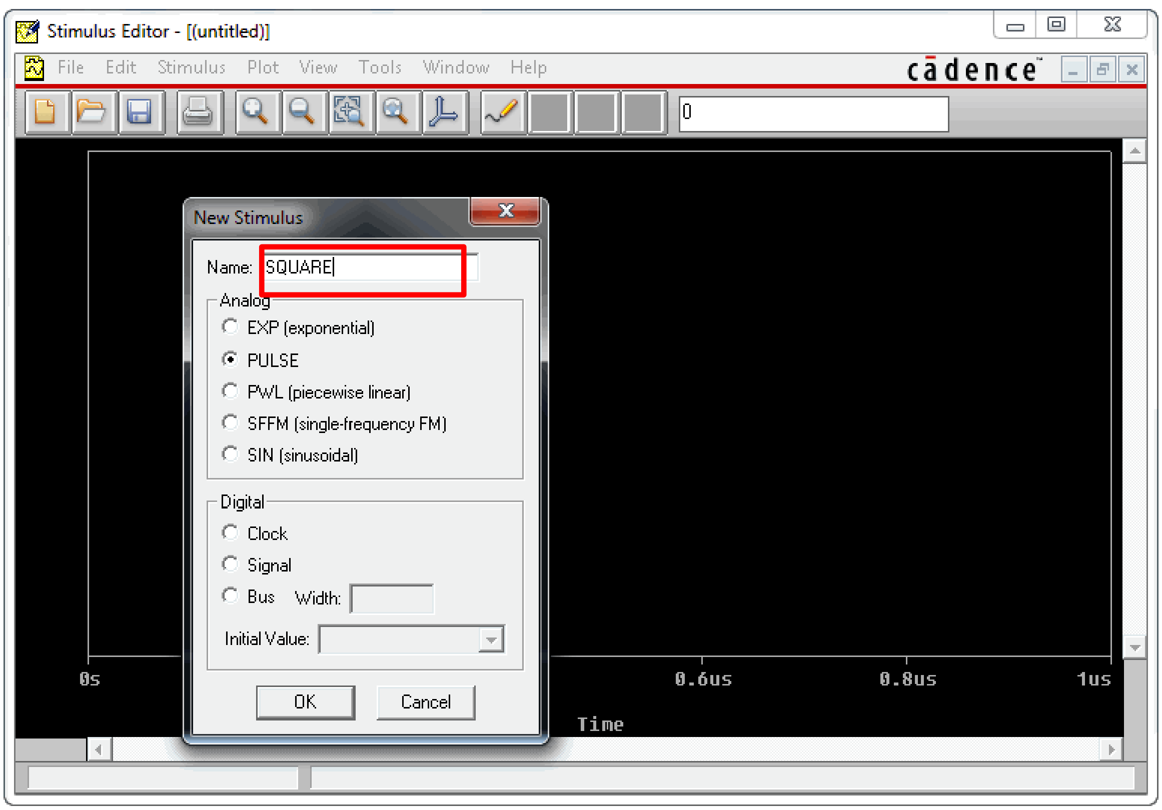


Figure 2-13: Defining stimulus name

14. Select the **PULSE** radio button in the **Analog** section of the **New Stimulus** form and click **OK**. The **Pulse Attributes** form is presented.

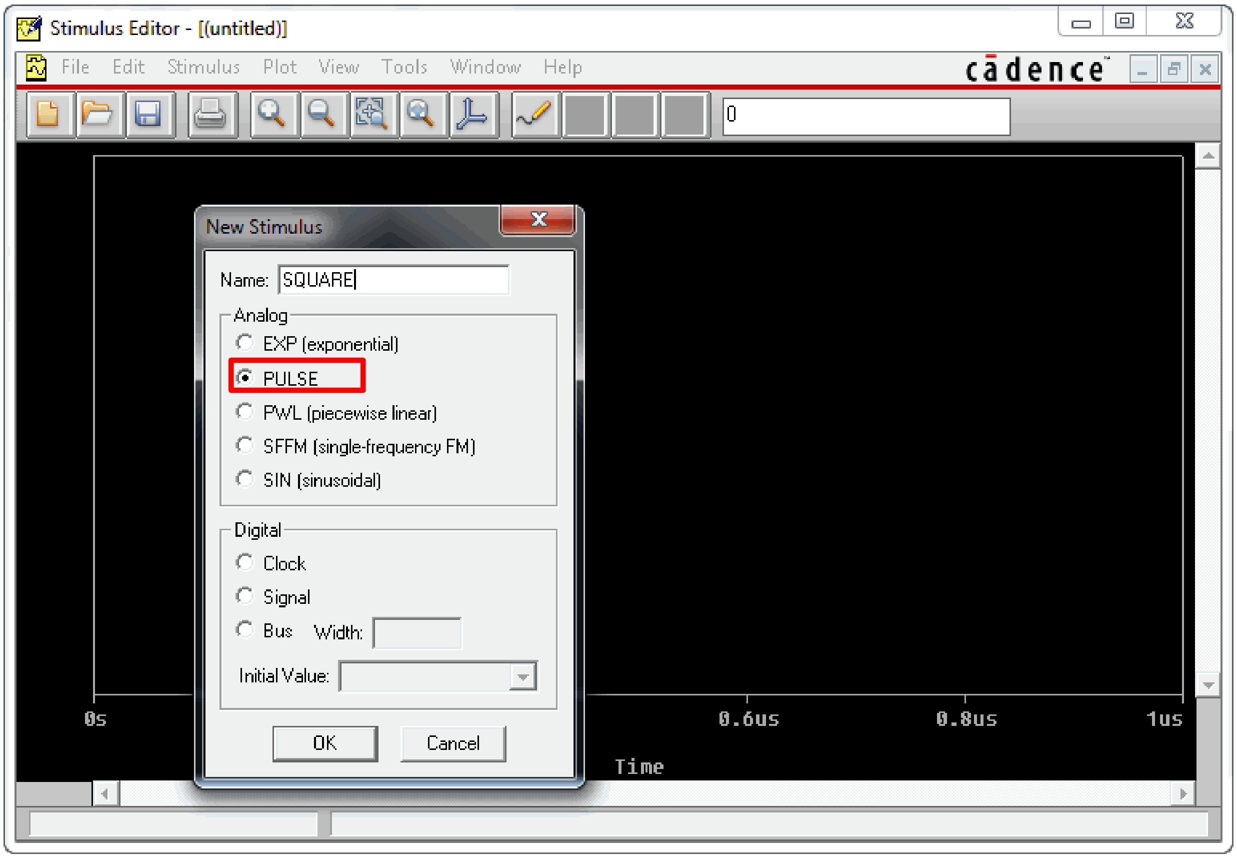


Figure 2-14: Defining stimulus type

15. You will define a 2V (peak amplitude) square wave with a period of 200us and 10us rise and fall times. Fill in the **PULSE Attributes** form, as shown in Figure 2-15 and click on **OK**.

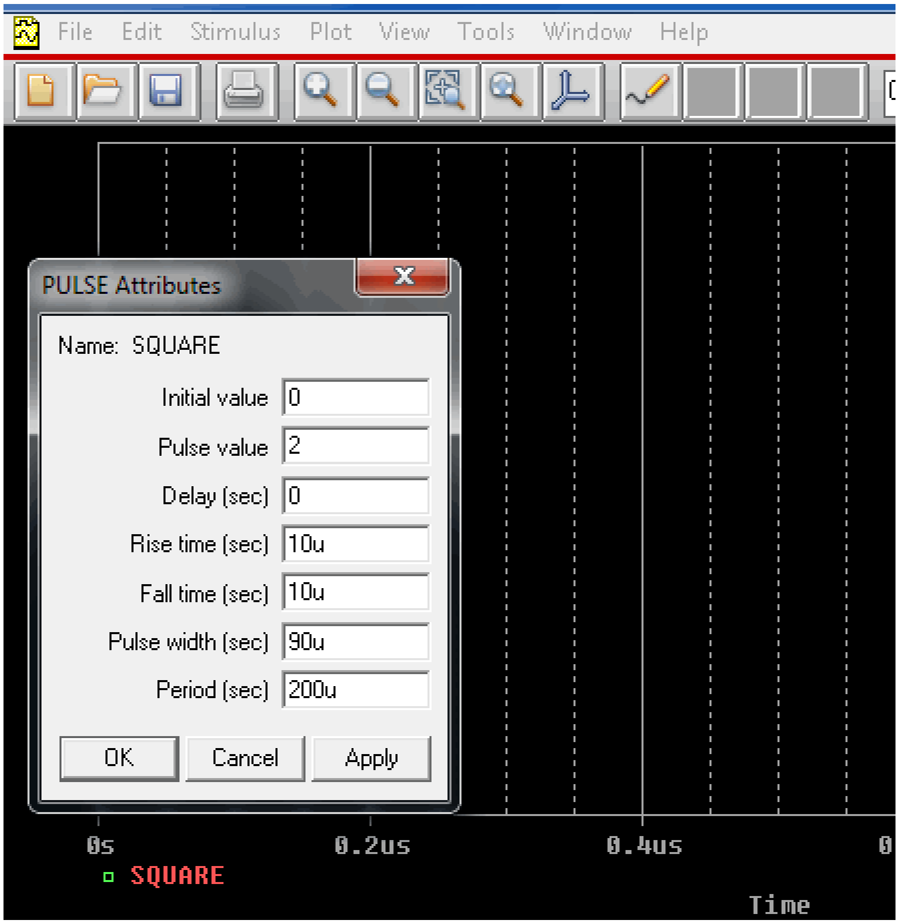


Figure 2-15: Pulse Attributes Settings

16. The **Stimulus Editor** now shows the SQUARE stimulus, as in Figure 2-16. Examine it in the context of the pulse attributes in Figure 2-15.

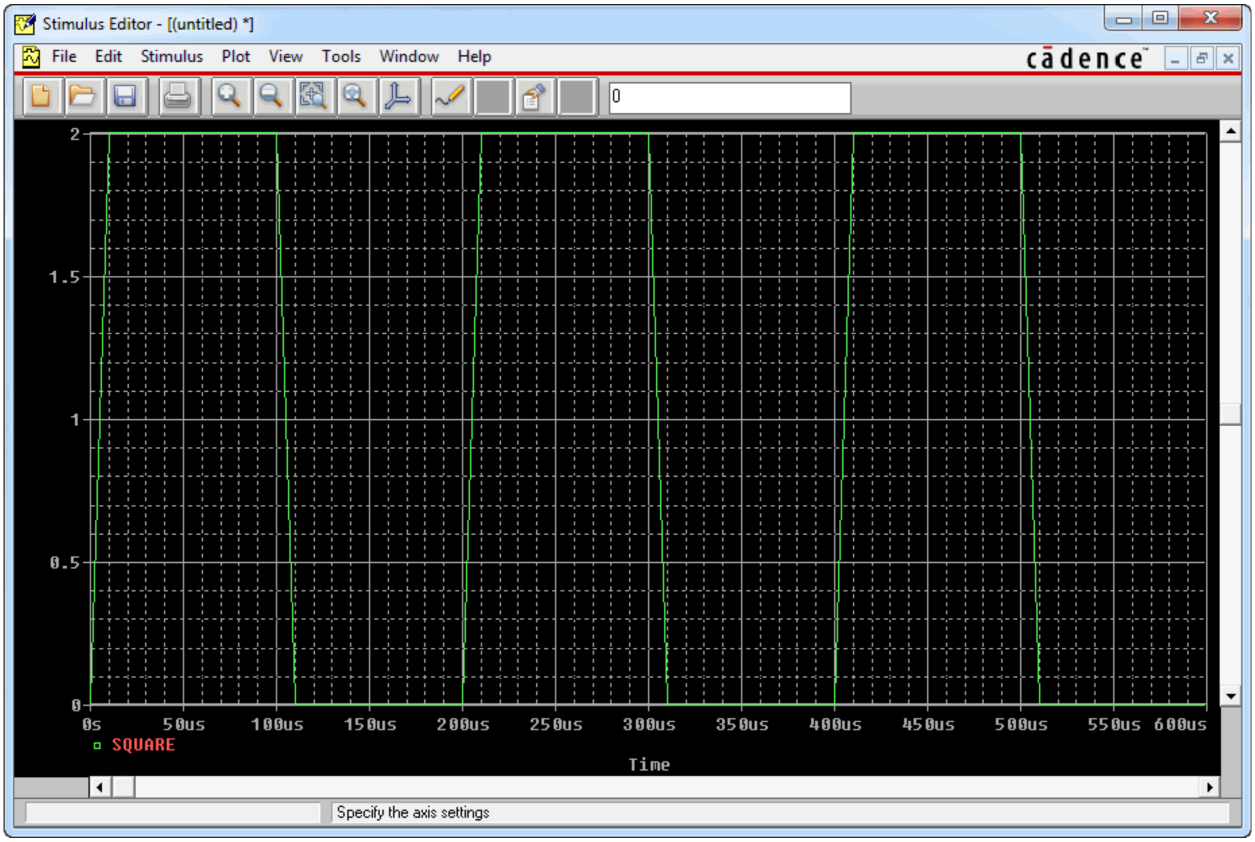


Figure 2-16: “Square” Stimulus Waveform

17. Save the stimulus (**File > Save As**), browse to the **module2** folder, and save `square.stl`.

18. Add the stimulus to the simulation by editing the Simulation Profile and selecting the **Configuration Files** tab.

19. Highlight the stimulus file. Browse to the location where you saved the SQUARE stimulus and add it to your design.

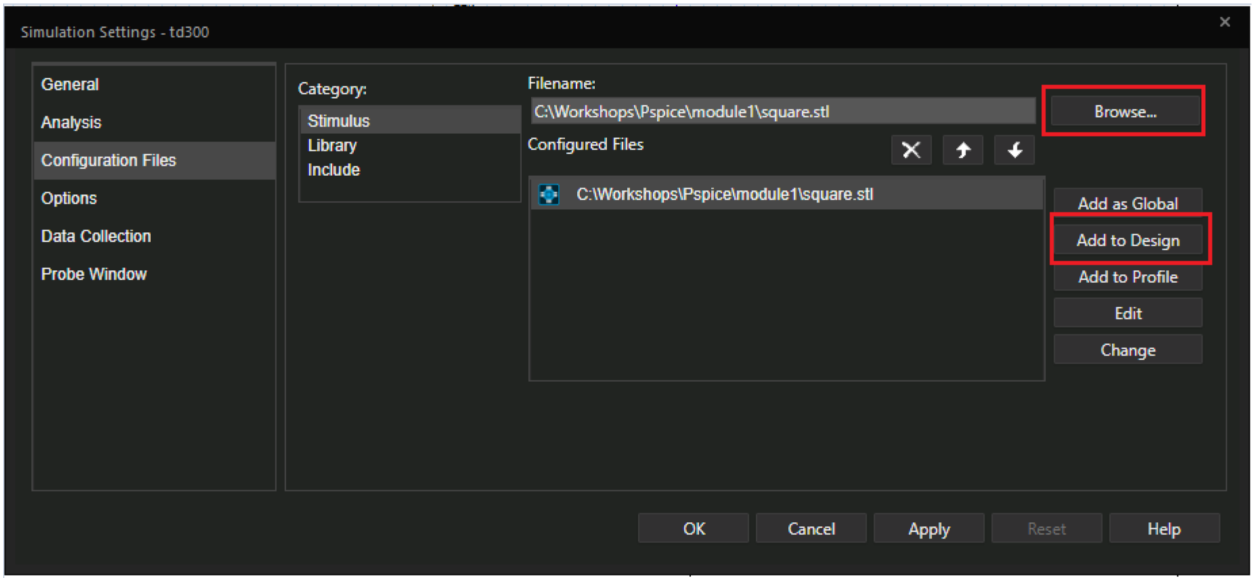


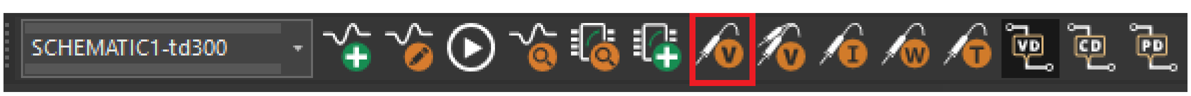
Figure 2-17: Adding stimulus to simulation profile

20. Close (**File > Exit**) the Stimulus Editor. The SQUARE stimulus in now defined.

Lab 6: Placing Voltage Probes

Although waveforms can be displayed in the PSpice Probe window without using the probe symbols placed on the schematic, the intuitive and familiar nature of the probes make them essential in specifying many measurements. Supported probe functions include voltage, current, power, differential voltage, as well as powerful advanced/template probes that allow easy instantiation of predefined plot configurations, such as Bode plots. You will place a couple of voltage probes in this exercise.

21. Select the Voltage Probe in the analog toolbar and place one each on the IN and OUT wires (see Figure 2-18). The requirement for placing probes is that voltage probes are connected to wires, current probes are connected to a component pin's connection point, and power probes are placed directly on the body of the part.



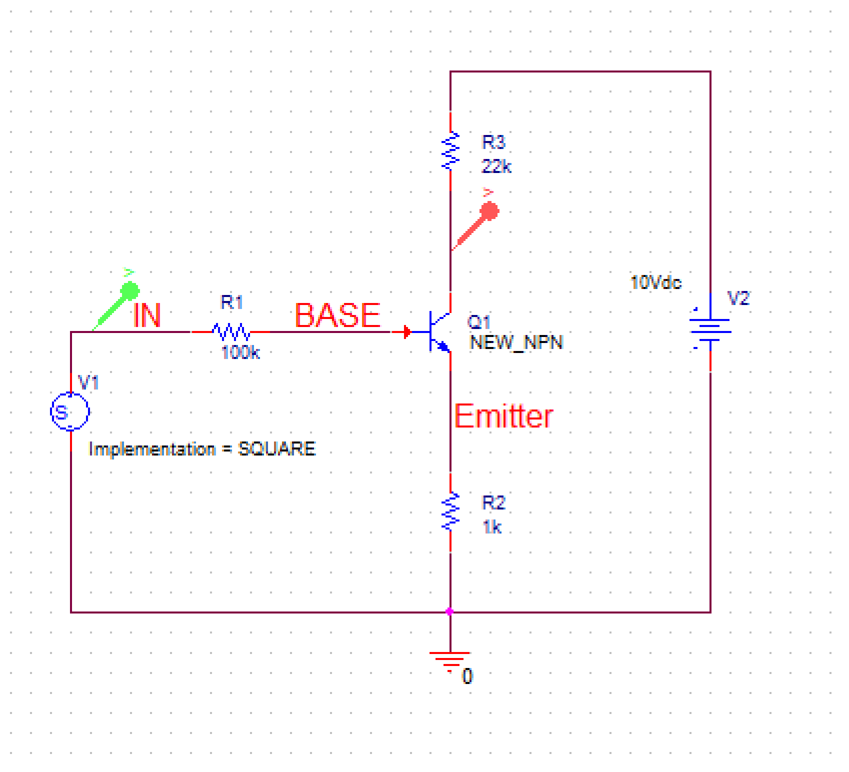


Figure 2-18: Voltage Probes Placed

22. Save the design.

Your design is now ready to simulate.

Lab 7: Simulating the Design

23. Select the Simulate (Run PSpice) button from the Analog toolbar OR select the **PSpice > Run** menu. Select **Yes** to save the design if prompted.

24. The above action triggers the following events:

    a. The netlist is (re)generated, as necessary.

    b. PSpice is invoked and its window opens.

    c. The netlist, the “td300” simulation profile, and the probe information are submitted to PSpice.

    d. A simulation is run using the profile settings.

e. The probe displays the simulation progress and the resulting waveforms.

Note that the trace symbols and colors in Figure 2-19 may not match your results.

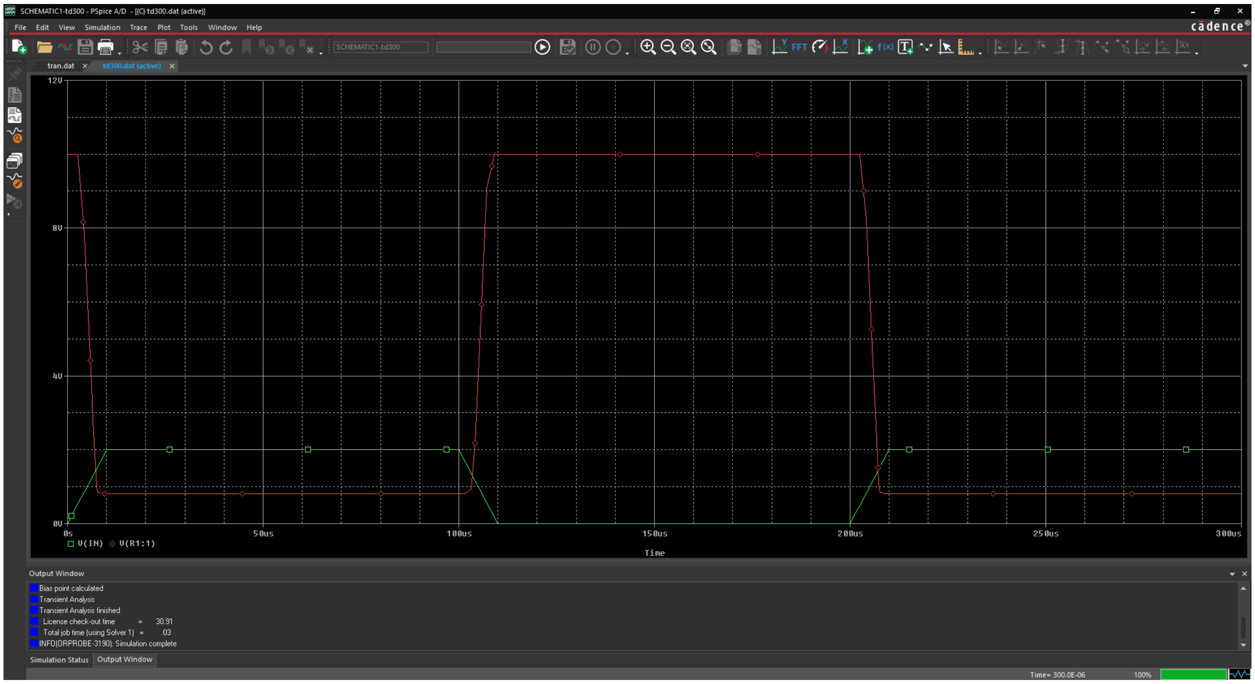


Figure 2-19: Simulation Results in Probe

Lab 8: Customizing the Probe Window

The Probe is the PSpice output tool that allows you to view both time- and frequency-domain analysis using a single window. With Probe, you will be able to define traces and apply measurements to extract design-critical data. In the preceding sections, you will learn how to use Probe to view and analyze waveforms that are critical to your design.

25. It may be useful to have the waveform window have visual precedence over all other windows. To do this, select the **Always On Top** button on the left of the Probe window or select **View > Always On Top**. It functions as its name would imply. It can be toggled depending on your preference. The icon is outlined when active.

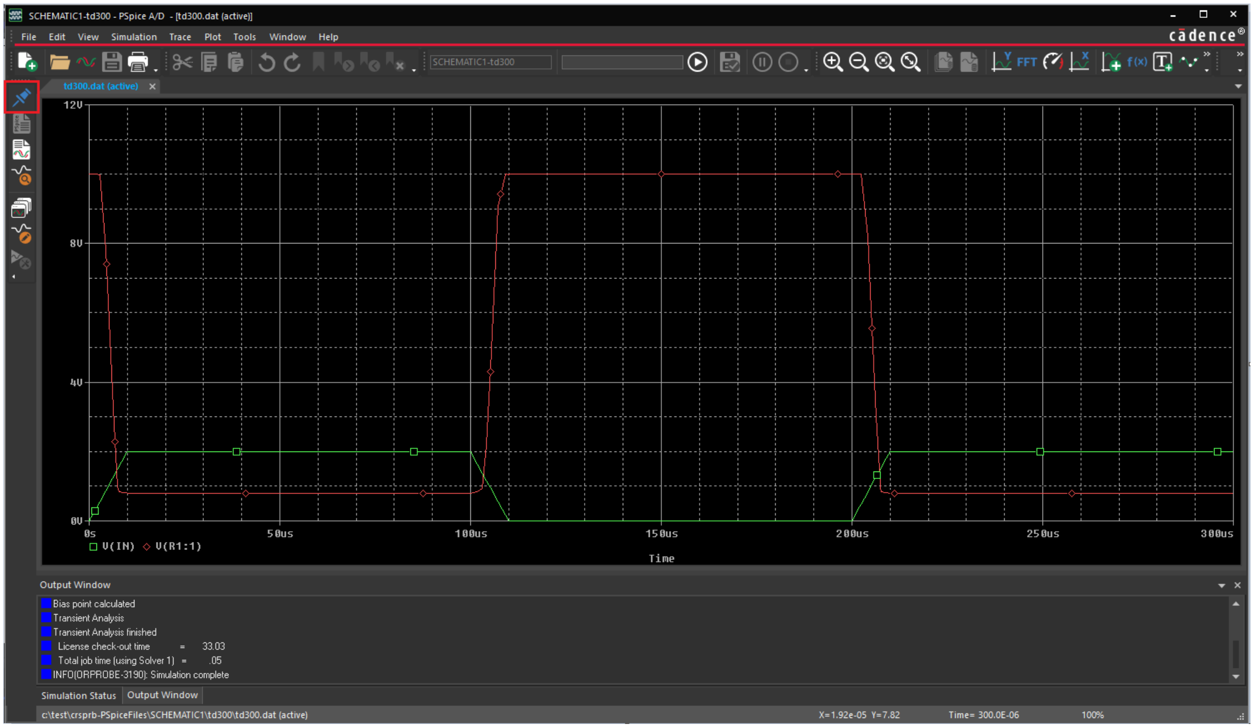


Figure 2-20: Turning on the "Always On Top" mode

26. Deselect (turn off) the 'Always On Top' mode if you wish.

27. In Probe, select **View > Alternate Display** to activate the Alternate Display mode.

    By default, Alternate Display shows only the waveforms and menus and is set to be "always on top", but each of the two display modes is equally configurable. The display configuration is customized largely using the **View** menu options.

28. Resize and position the window as desired for this view. Do not deactivate the Alternate Display mode or the Always on-top mode (which is now only accessible through the View menu).

29. Double-click in the left margin of the Probe window to invoke the Axis Settings form, as shown in Figure 2-21.

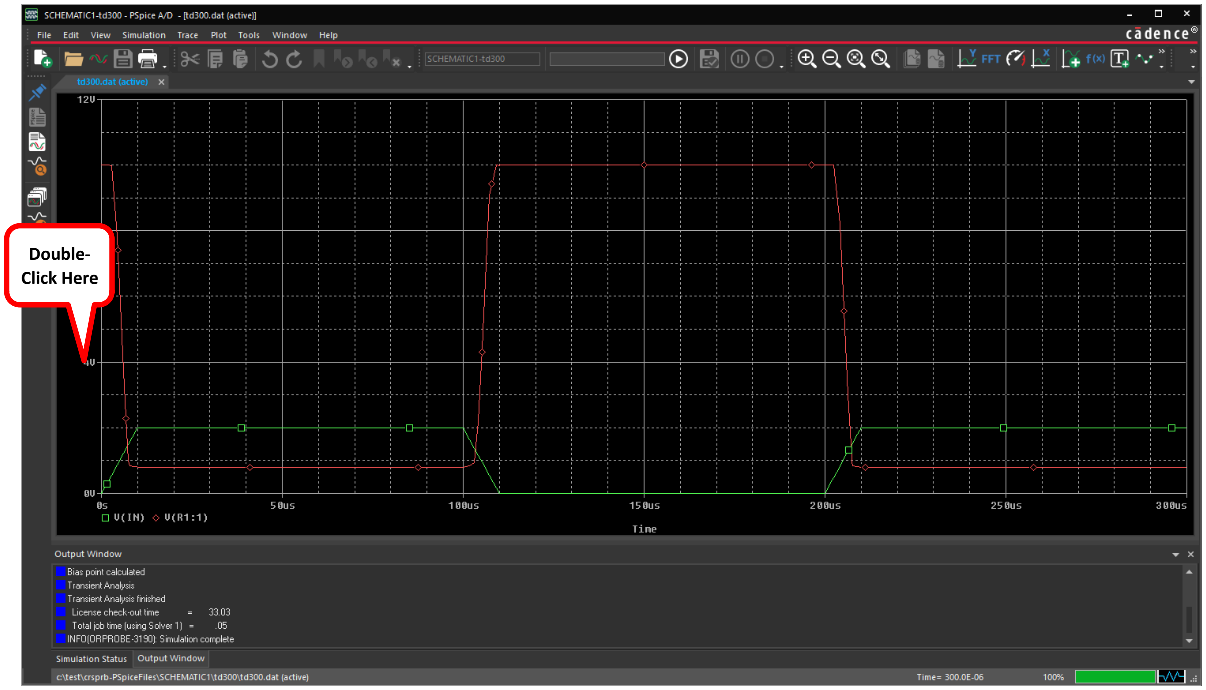


Figure 2-21: Alternate Display Mode

30. Configure the **Data Range** section to match Figure 2-22 for improving the Y-axis range. This will fix the displayed voltage range so that the following steps will not make undesired changes as you select different nodes for display in Probe.

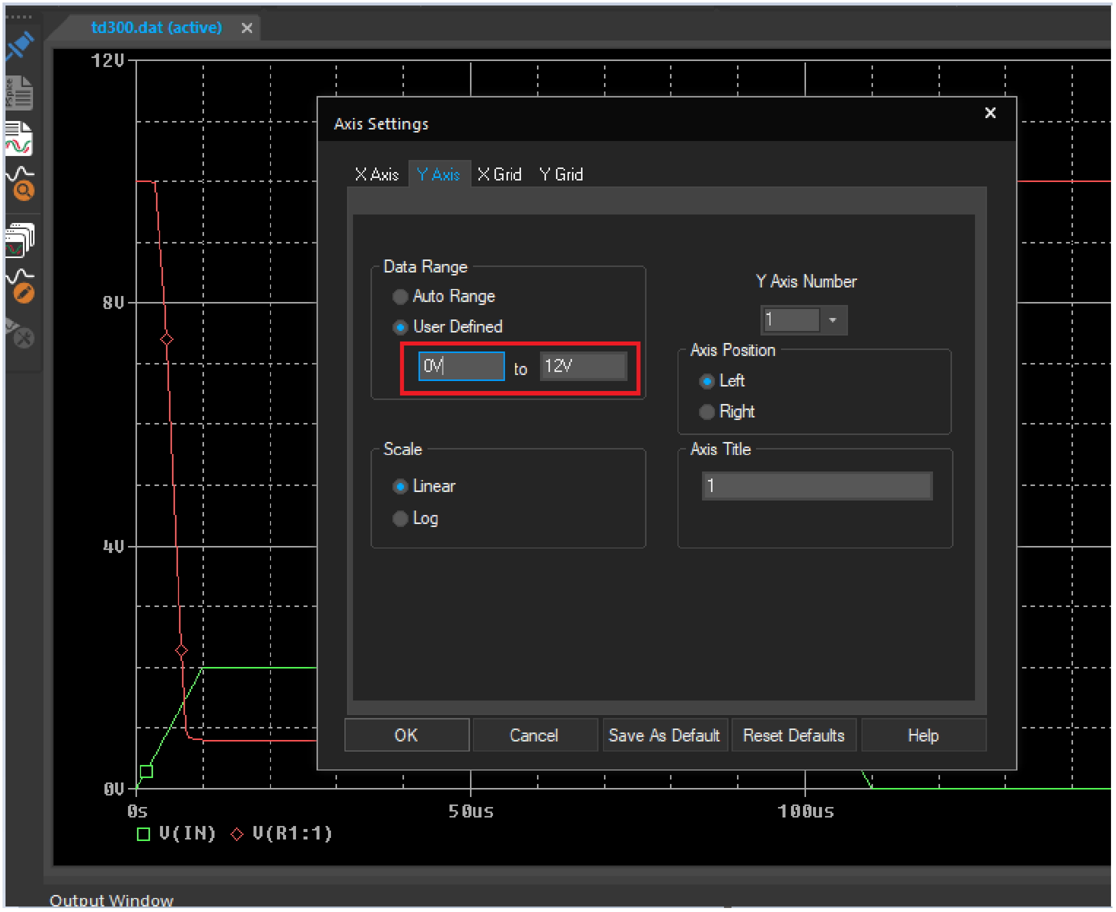


Figure 2-22: User-Defined Axis Settings

31. Select the **OK** button on the **Axis Settings** form. If your displayed voltage scale did not previously match Figure 2-22, it should now.

32. Position the Capture and Probe windows so that you can see a good portion of the schematic (with focus on the transistor) as well as a portion of the waveforms. As configured, the Probe window should always be in front of Capture.

33. In Capture, move the voltage probe from the **OUT** wire to the **BASE** wire and note that the waveform in Probe is immediately updated to reflect the new probe location, but the voltage scale remains at 0-12V.

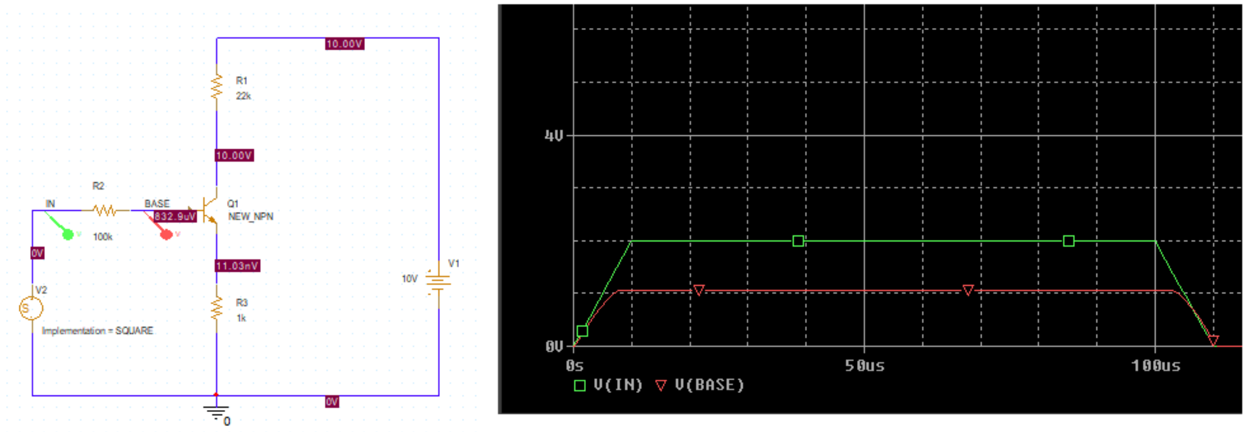


Figure 2-23: Repositioned Voltage Probe and Updated Probe Window

34. Return the Voltage Probe to the OUT wire.

Lab 8: Adding Traces to Probe Window

Probes are a handy and powerful tool in the PSpice flow as they automatically display the desired information in Probe with no required configuration. However, it is also desirable to be able to add traces to and configure the Probe window without the use of probes (particularly on multi-page designs, where all of the probes cannot be simultaneously seen) in such a way that the configuration is persistent from one session to the next.

35. Select the Add Trace button or select **Trace > Add Trace** to invoke the Add Traces form.

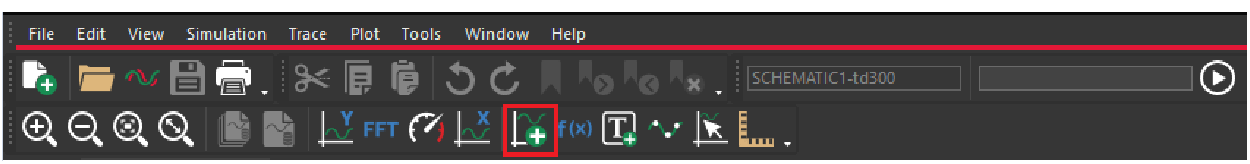


Figure 2-24: Adding a trace

36. Configure the filters for **Analog**, **Voltages**, and **Alias Names**, as shown in figure 2-25. Filters allow you to control the information that is displayed in the **Add Traces** form.

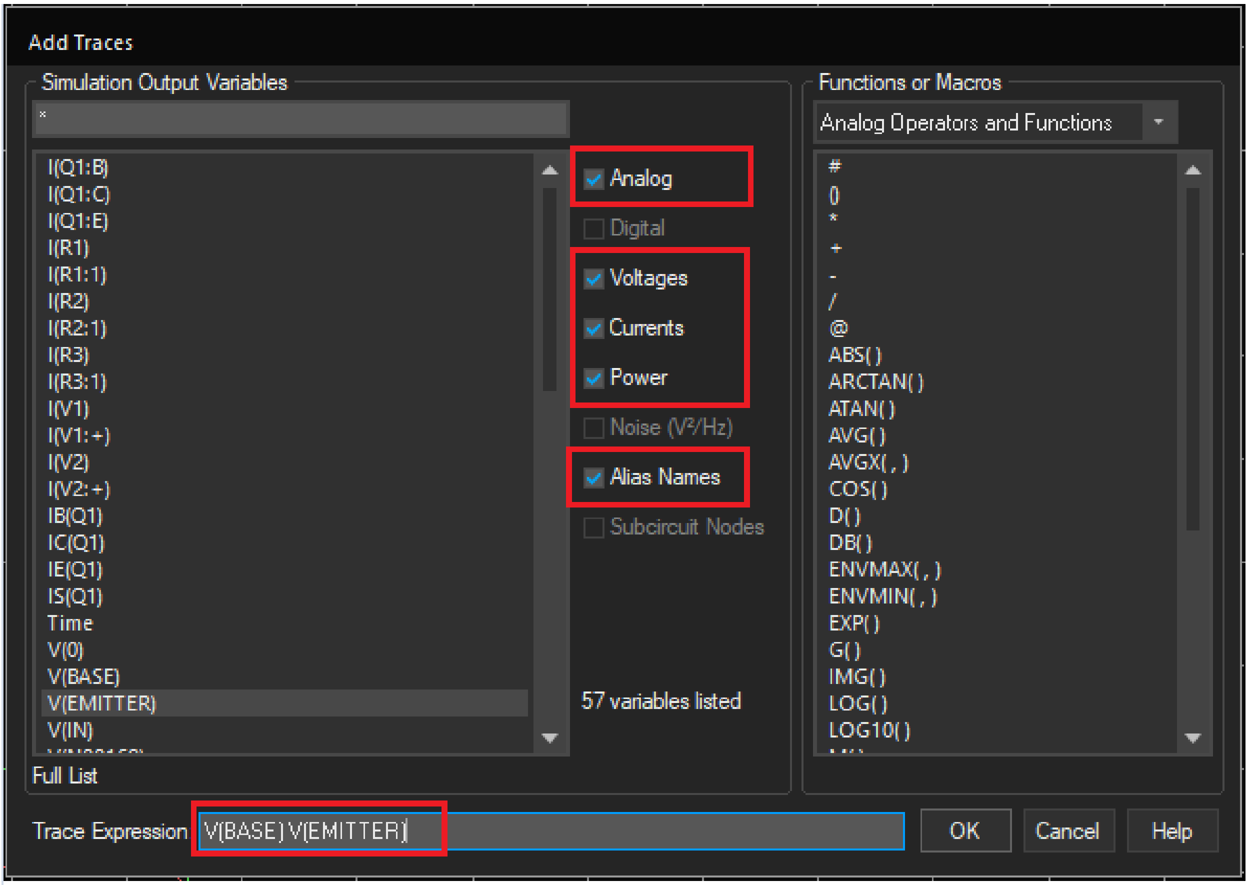


Figure 2-25: Adding V(BASE) and V(EMITTER) traces to Probe

37. Select **V(BASE)** from the list on the left, followed by **V(EMITTER)**.

    The two expressions are populated into the **Trace Expression** field at the bottom. This specifies <u>two</u> different traces to be added. If there were a mathematical operator (like '+') between the two voltages, they would be treated as parts of a single larger expression and trace to be displayed.

38. Select **OK** to add the two traces to the Probe waveform window. The waveforms should now match Figure 2-26; trace colors/symbols may differ.

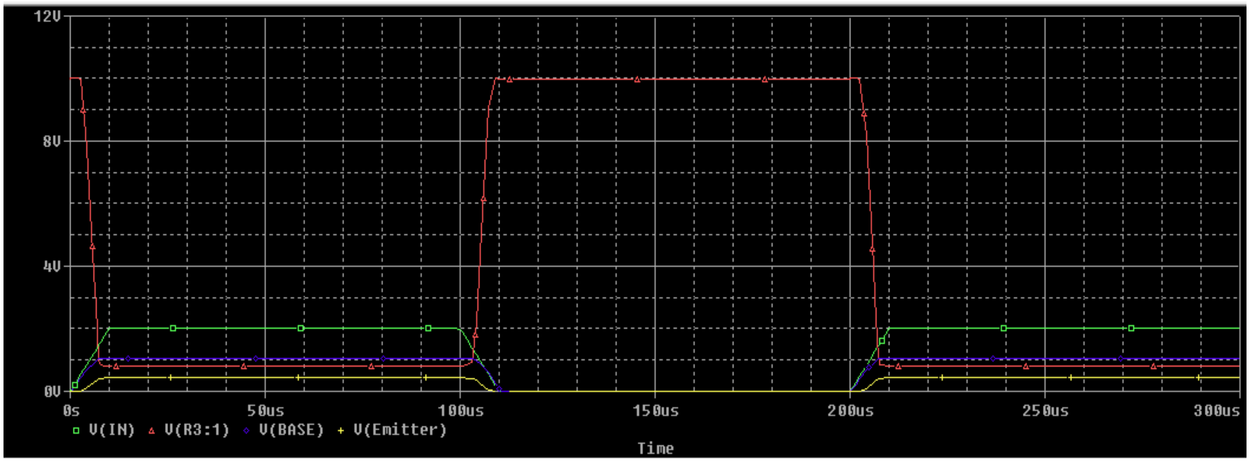


Figure 2-26: Four Traces in Probe

You have added two traces in Probe, but if a simulation were rerun, you would lose the newly added traces because the simulation profile is configured to display the probed traces. You need to fix this.

39. Close the Probe Waveform window. This commits the current trace layout to the simulation profile memory.

40. In Capture, select **PSpice > Edit Simulation Profile**.

41. In the Probe Window tab, select **Last Plot** to instruct Probe to reuse the most recent trace configuration in the next simulation.

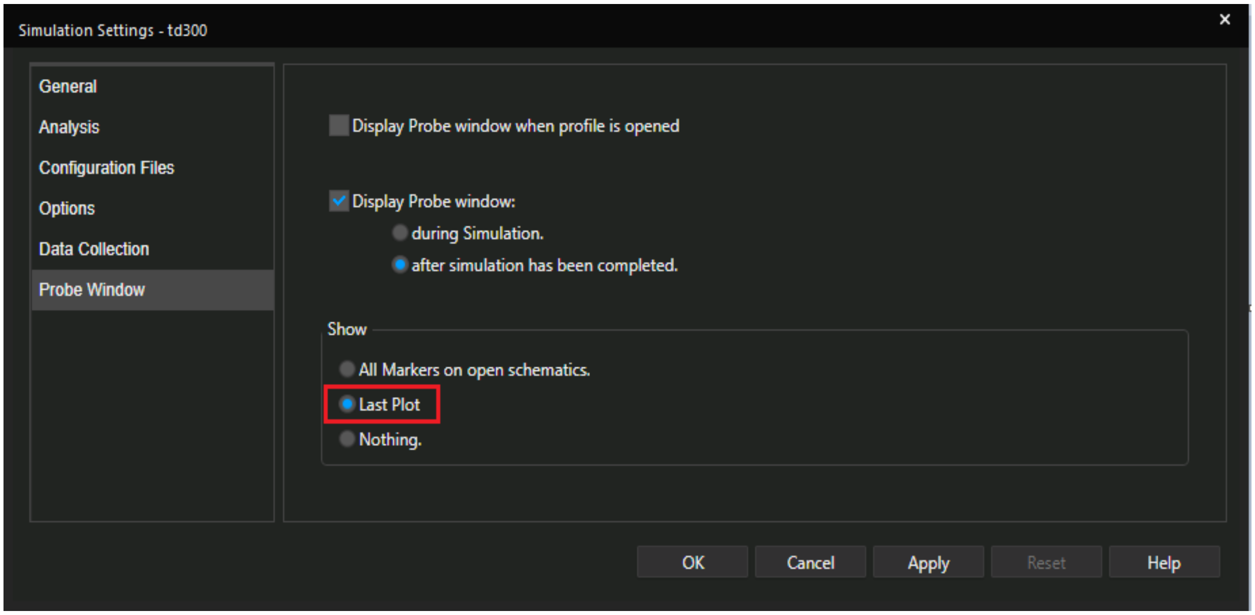


Figure 2-27: Last Plot

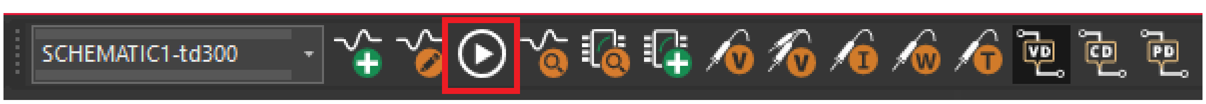
42. Select **OK** in the **Simulation Settings** form.

    At this point, the probe symbols on the schematic are no longer needed.

43. Delete the two probes (on wires IN and OUT) on the schematic. Select and use the **Delete** key.

44. Save the design.

45. Simulate the design. Note that the previous trace arrangement has been retained. This would be the case even if the project were closed and reopened on a later day, or if other simulation profiles had been created/utilized before returning to the td300 profile.



Lab 9: Basic Waveform Measurements

To demonstrate the use of Probe cursors in making waveform measurements, you will perform a simple differential voltage measurement against the current simulation results. You will measure the approximate maximum voltage across the base resistor during the falling portion of V(in).

46. Select the **Zoom Out** button to cancel out of the fixed Y scale and zoom out.

47. Select the **Zoom Area** button in the Probe window and drag-select across the area shown in Figure 2-28 initially, and then adjust by additional scroll/zoom so that the displayed area resembles that of Figure 2-28.

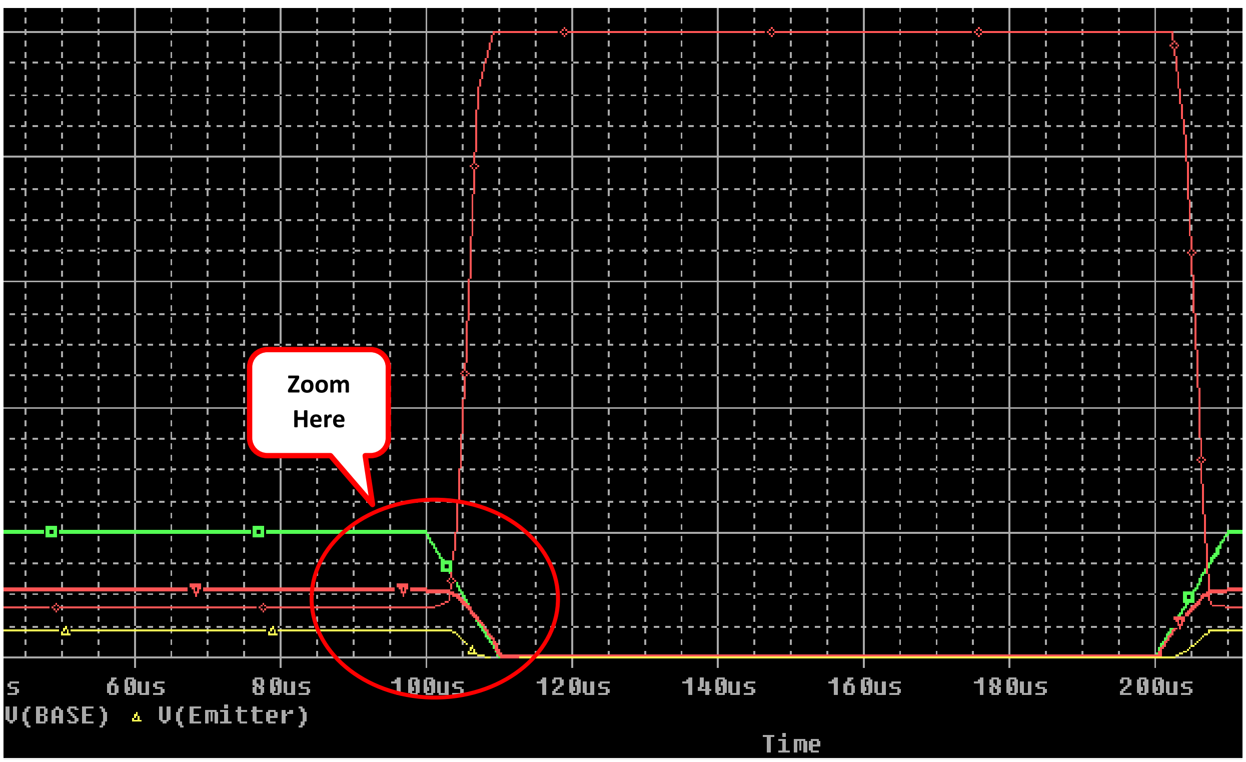


Figure 2-28: Zoom Area

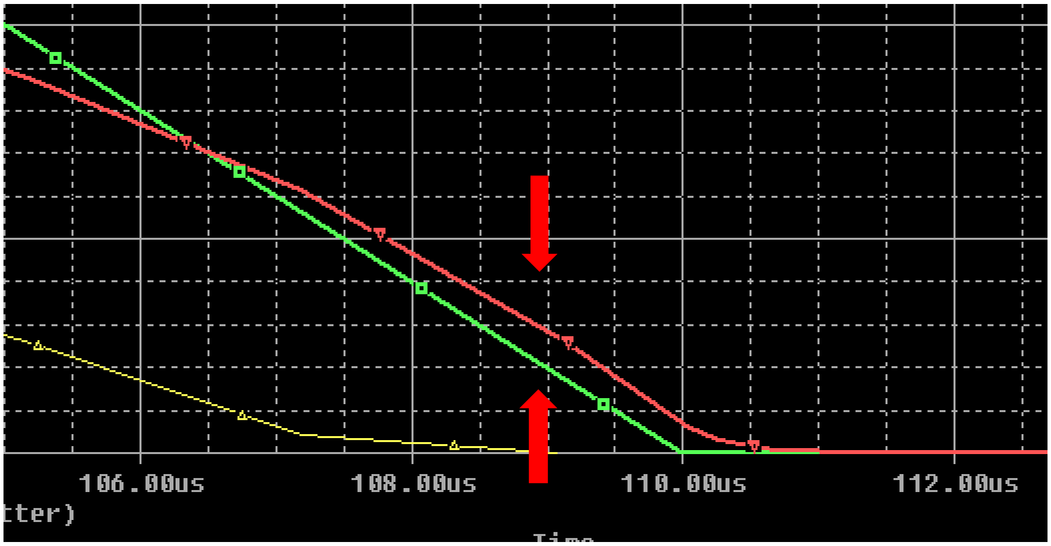
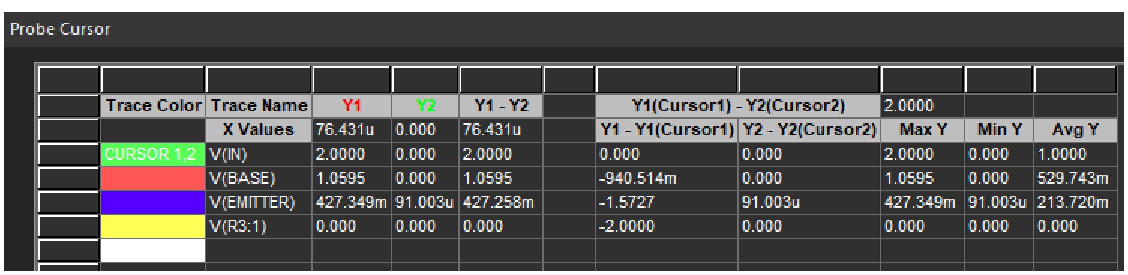


Figure 2-29: Zoom Results V(base) exceeding V(in) by 85-90mV

In the measurement exercise, you want to find the maximum excursion of V(base) beyond V(in), which is caused by the transistor's base charge and collector-base leakage. Thus, you want to measure the vertical (voltage) difference between the two traces somewhere in the area of the arrows in Figure 2-29. You will do this by activating the trace cursors and configuring them to track the V(base) and V(in) traces as they are manually moved horizontally across the waveform plot.

48. At the top of the Probe window, select the Toggle Cursor icon to enable the cursors. The Probe Cursor window opens as in Figure 2-30, displaying data for all four traces. It currently indicates that both cursor1 and cursor2 are associated with V(in). Next, you will associate the cursors with the proper traces.


Probe Cursor

Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		2.0000		
	X Values	76.431u	0.000	76.431u		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	V(IN)	2.0000	0.000	2.0000		0.000	0.000	2.0000	0.000	1.0000
	V(BASE)	1.0595	0.000	1.0595		-940.514m	0.000	1.0595	0.000	529.743m
	V(EMITTER)	427.349m	91.003u	427.258m		-1.5727	91.003u	427.349m	91.003u	213.720m
	V(R3:1)	0.000	0.000	0.000		-2.0000	0.000	0.000	0.000	0.000

Figure 2-30: Cursor Window

49. At the lower-left corner of the waveforms (the Legend; see Figure 2-31), left-click on the **symbol** for **V(base)** (shown as a triangle in the figure; your plot may differ). A

fine-dotted pattern will surround the symbol – this indicates that cursor1 is now associated with and will track V(base).

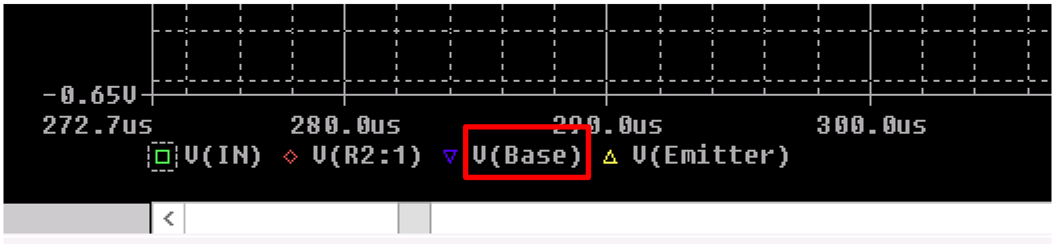


Figure 2-31: V(base) tagged for cursor tracking

50. To similarly associate cursor2 to **V(in)**, right-click on its **symbol** (shown here as a square).

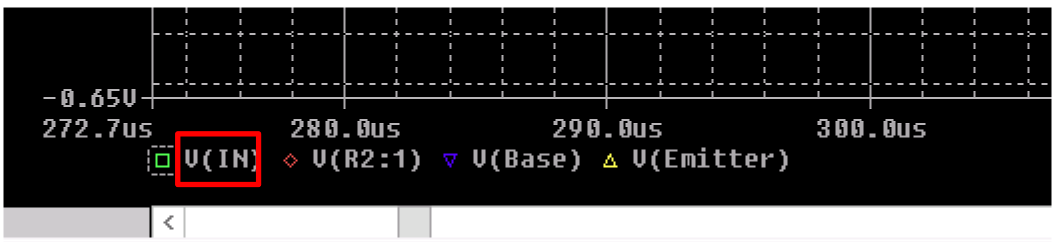


Figure 2-32: V(in) tagged for cursor tracking

Selecting anywhere in the waveform area with the left or right mouse button will now track the associated trace because each button is now linked to its own trace.

51. Left-click and hold the mouse button while moving it across the canvas until cursor1 (red) is upon the area with the greatest apparent vertical distance (voltage) between the two traces.

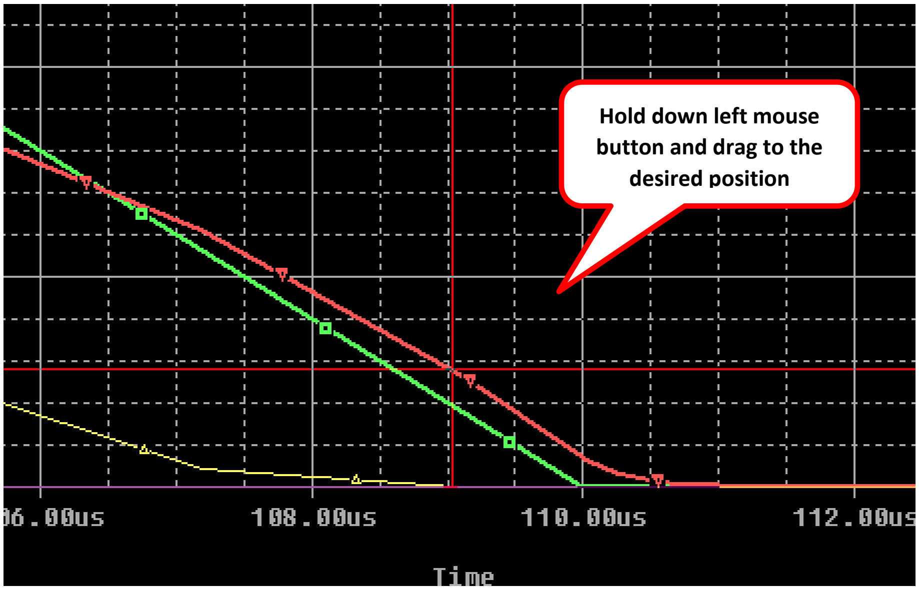


Figure 2-33: Setting cursor1 position

52. Without moving the mouse significantly, right-click to place cursor2 (green) at the same horizontal (time) position.

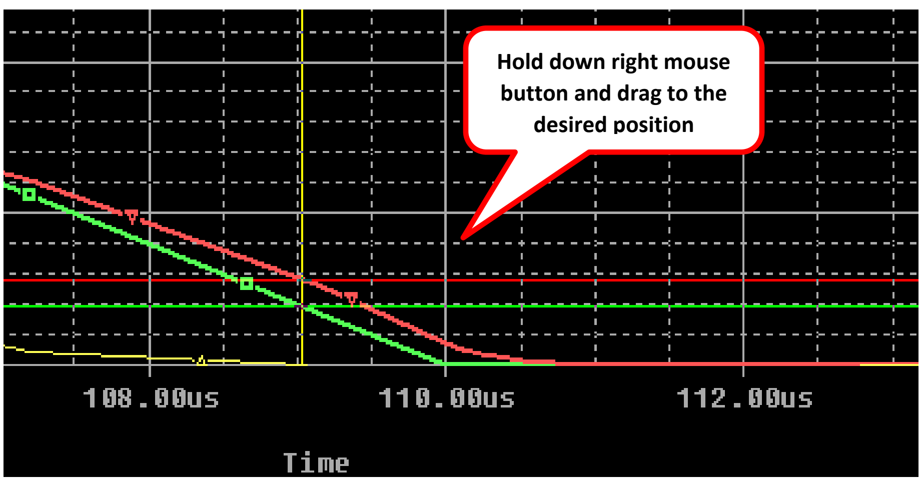
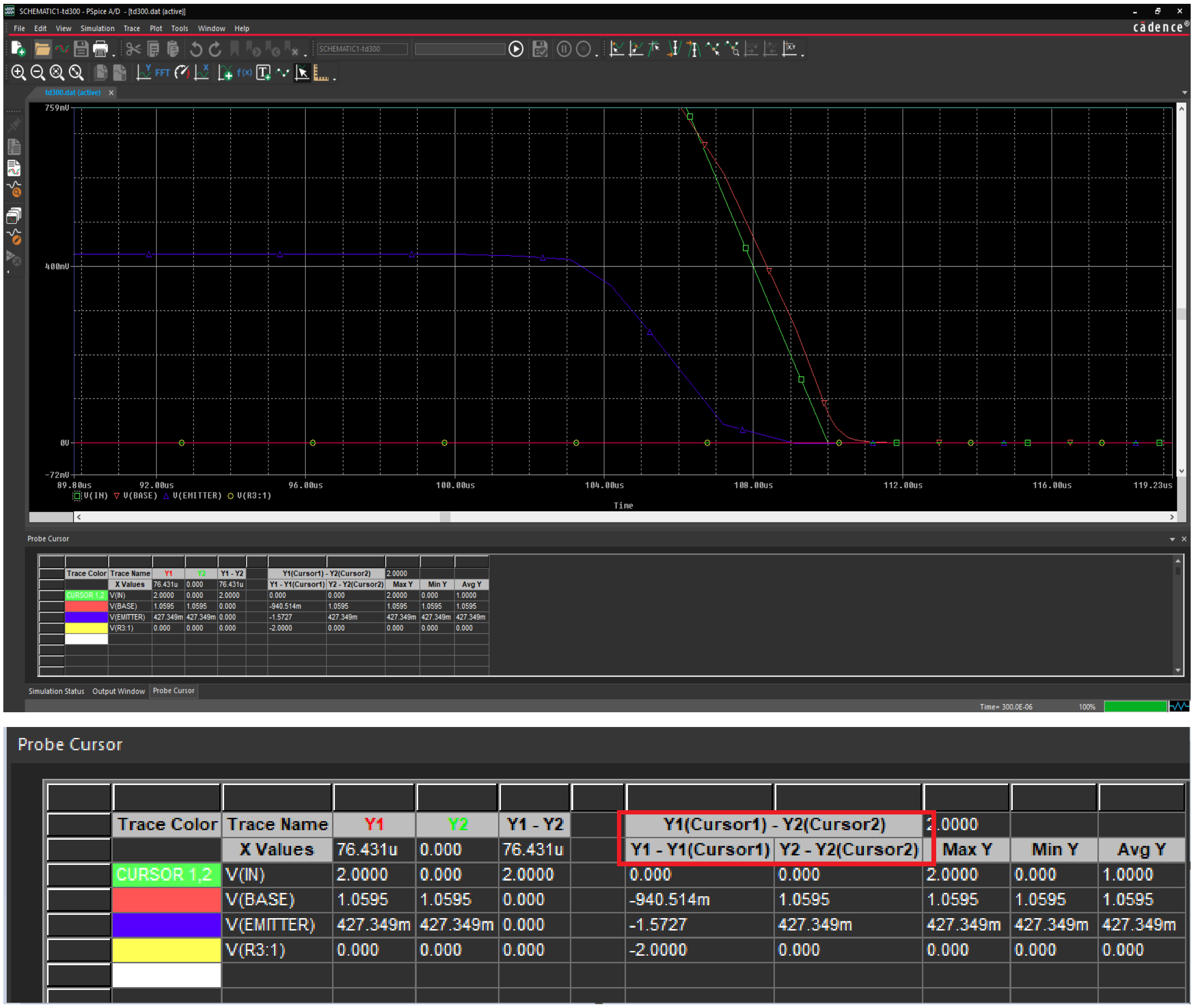


Figure 2-34: Setting cursor2 position

53. Note the probe cursor data, as shown in Figure 2-35. The Probe Cursor Display reports the absolute and relative position of cursor1 and cursor2, as well as a wealth of additional values related to cursors and traces. The data you seek is a maximum in the encircled value in Figure 2-35. This field represents the Y (voltage) difference between the two cursors on their respective traces.



	Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		2.0000		
		X Values	76.431u	0.000	76.431u		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	CURSOR 1,2	V(IN)	2.0000	0.000	2.0000		0.000	0.000	2.0000	0.000	1.0000
		V(BASE)	1.0595	1.0595	0.000		-940.514m	1.0595	1.0595	1.0595	1.0595
		V(EMITTER)	427.349m	427.349m	0.000		-1.5727	427.349m	427.349m	427.349m	427.349m
		V(R3:1)	0.000	0.000	0.000		-2.0000	0.000	0.000	0.000	0.000

Figure 2-35: Measurement using the A1 and A2 cursors

54. Reposition the cursors horizontally by simultaneously holding the left and right mouse buttons and panning left/right to find the maximum reported differential voltage. This should be at the coordinates shown in Figure 2-35 – reporting a voltage difference of about 87mV.

For those who are used to the older style cursor display or may need a more compact view of the basic cursor differences, this can be enabled in **Tools > Options > Cursor Settings**. This form also allows color adjustments and other features to the cursors.

You have made some manual measurements using the cursors to find the maximum voltage difference between the two traces. There are ways of automating this type of process in the PSpice simulator. You will briefly cover them both.

Lab 10: Assertions

Assertions are a feature of PSpice's "Arbitrary Source" analog behavioral models. They allow you to define an expression, which if met during a simulation run, will produce a runtime customized warning or an error message. You will use the **CURRENT_GEN** part from the **Function** library to instantiate this feature for this exercise, as it requires no support components to serve this purpose. The error/warning parameters (the important parameters) will be defined in the steps given below.

55. In Capture, open a design page and select the **Add Component** button.

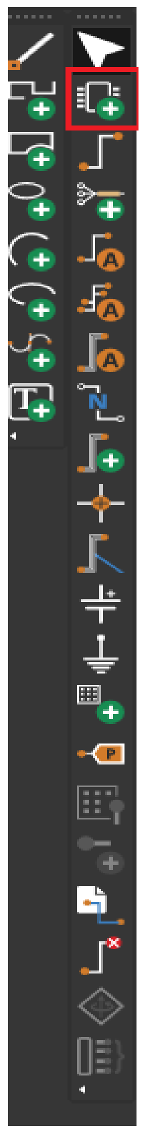


Figure 2-36: Placing a component

You will add the **Function** library to the available list of libraries within Capture.

56. In the **Place Part** window, select the **Add Library** button.

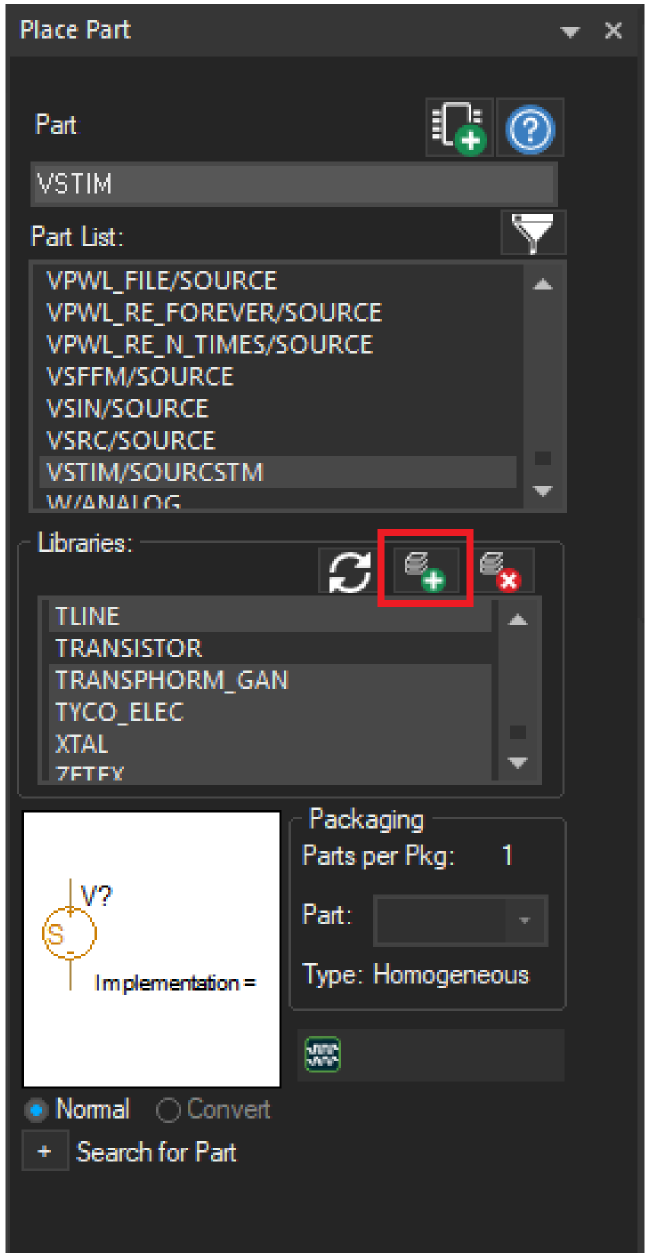


Figure 2-37: Adding the Function library

57. Browse to the Function library available at **C:\Cadence\SPB_17.2\tools\capture\library\pspice\advanls**.

58. Place the **current_gen** part on the schematic by following these steps:

    a. In Place Part, select the **FUNCTION** library.

b. Choose the **CHARGE_GEN** component and double-click the component image.

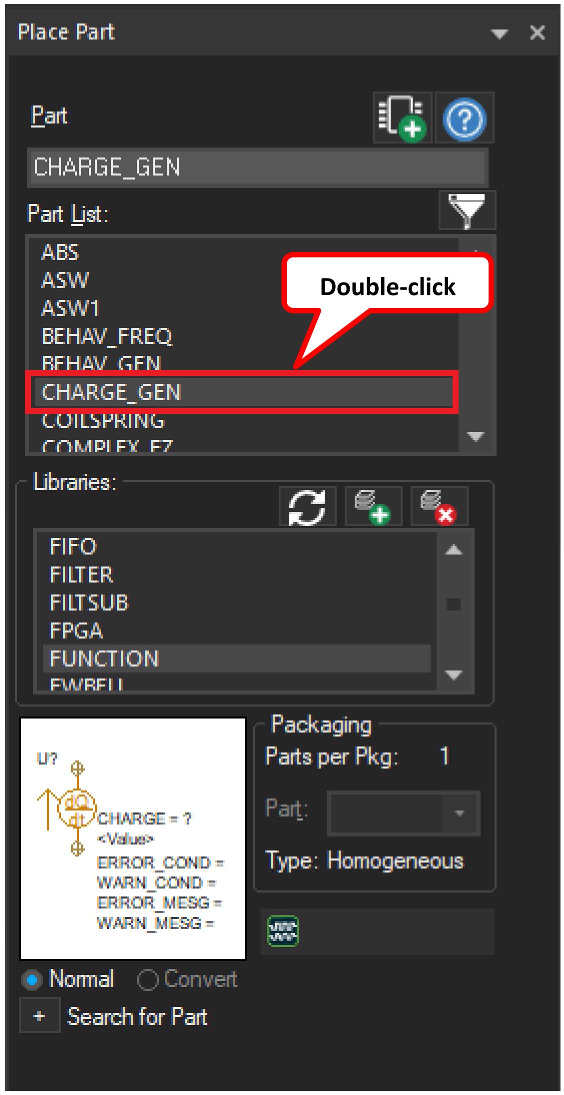


Figure 2-38: Selecting CHARGE_GEN

c. Place it in the lower right of the design, as shown in Figure 2-39, and right-click **End Mode**.

59. Wire the **current_gen** part, as shown in Figure 2-39.

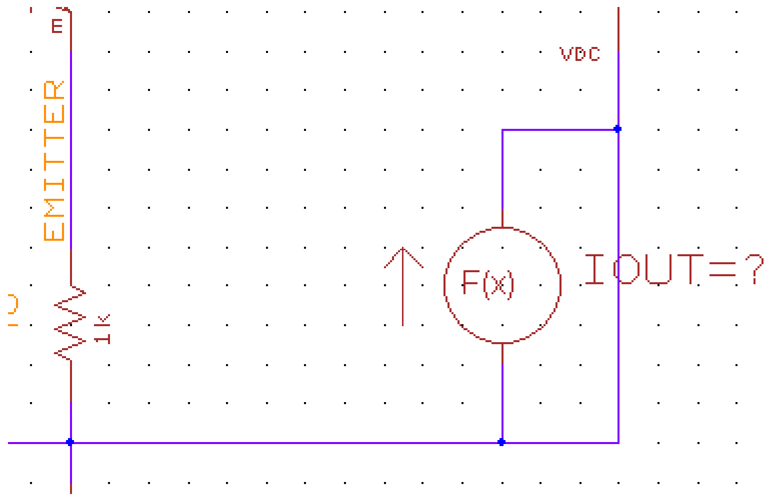


Figure 2-39: The current_gen part placed and connected

60. Save the design (**File > Save**).

    You will now edit the attributes of this part to configure it so that it will flag occurrences of V(base) exceeding V(in) by more than 80mV.

61. Double-click on the newly placed part to bring up the Property Editor.

62. Perform the following property edits using the Property Editor. When done, the two attributes for warning and error message should match Figure 2-40.

    a. Set the value of IOUT to 1.

    b. Enter **V(BASE) > V(IN)+80M** for the value of **WARN_COND**. This tests for V(base) exceeding V(in) by 80mV or more.

    c. Enter **Condition_Met** for the value of **WARN_MESG**.

    d. Set **ERROR_COND** as **V(BASE) < -100**

63. Set the Display Format of **WARN_COND** and **WARN_MESG** to **Name and Value**. Set all remaining visibilities to **Do Not Display**, as shown in Figure 2-40. The order of attributes is not important.

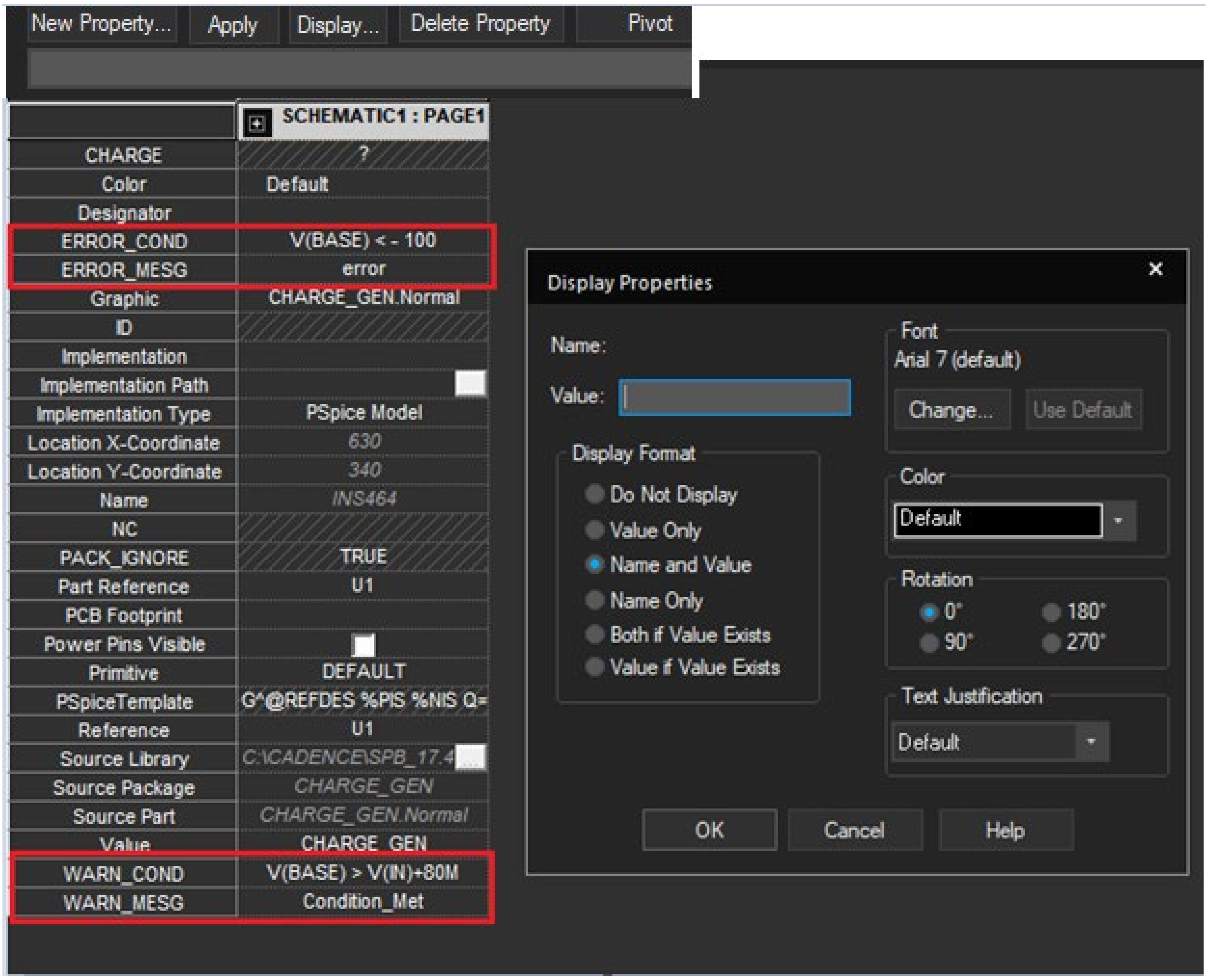


Figure 2-40: CURRENT_GEN Properties

64. Select Apply and exit the window.

65. Clean up the schematic so that it resembles Figure 2-41.

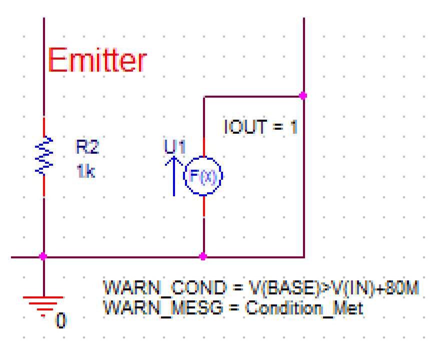


Figure 2-41: CURRENT_GEN placed and configured

66. Simulate the design (click 'Yes' to save).

Note the message "Condition_Met…" reported in the Output window, as shown in Figure 2-42. Also, because the "Last Plot" setting was selected in the simulation profile (step 41), the waveform plot layout (zoom, cursors, and so on) is not reset to the default but retains the prior configuration.

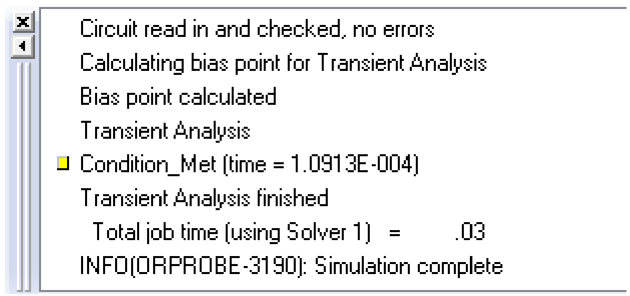


Figure 2-42: Assertion "Warning" Message

The reported event time matches the timepoint that was determined by your manual measurements in Figure 2-35 The usefulness of assertions as a runtime conditional test has been demonstrated. You will now measure waveform details using a third method.

Lab 11: User-Defined Measurement Expressions

User-defined measurement expressions or measurements allow you to define a mathematical expression that can be based on one or more aspects of the simulation results. The measurement will yield a single numeric value based on the current simulation results. Measurements are a foundation element of the PSpice Advanced Analysis functionality, which is the focus of Module 3 of this workshop. In the following steps, you will define/load two measurements that will accurately produce the results previously obtained using the manual <u>cursor</u> manipulation and the behavioral model <u>assertion</u> capability.

67. If you have accidentally closed the Probe window, reinvoke it by selecting the **View Simulation Results** button in the Capture Analog Toolbar. This will return the Probe window without running another simulation.

68. In **Probe**, select the **Evaluate Measurement** icon or select **Trace > Evaluate Measurement**.

The **Evaluate Measurement** form is presented, as shown in Figure 2-43.

69. Using Figure 2-43 as a guide, set variables filters for **Analog**, **Voltages**, and **Alias Names**.

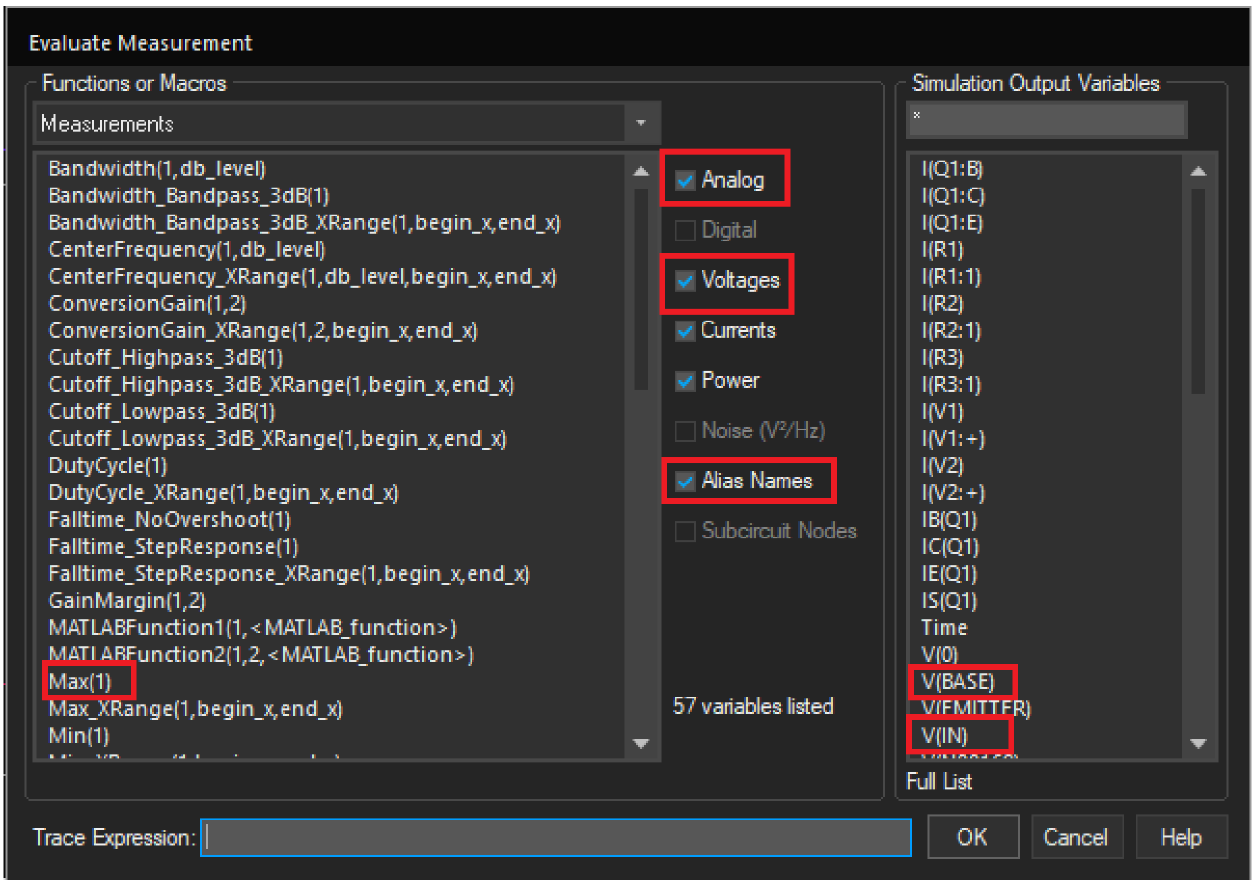
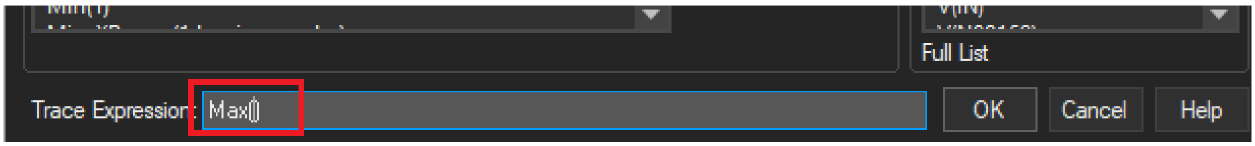


Figure 2-43: Probe Evaluate Measurement Form

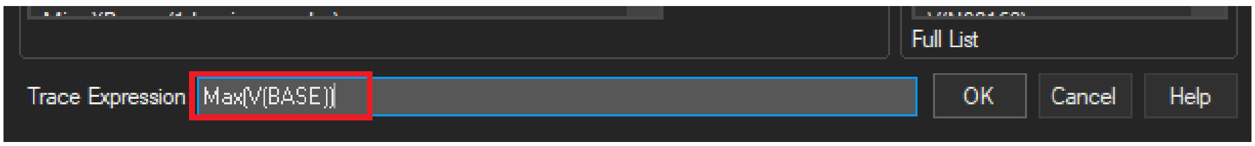
70. Referring again to Figure 2-43, perform the steps given below to create the first measurement, which will identify the maximum voltage difference that occurs (over the simulation period) between V(base) and V(in). <u>Be careful not to double-click during this process</u>.

    a. Left-click <u>once</u> on Max(1).

Note: Here, (1) means that the Max function is expecting a single numeric expression within its parenthesis. The cursor is automatically seeded in between them.

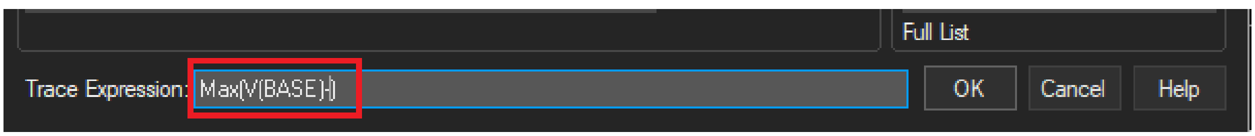


b. Left-click on **V(base)**. It is inserted in between the parenthesis. Do not worry about upper/lower-case differences.

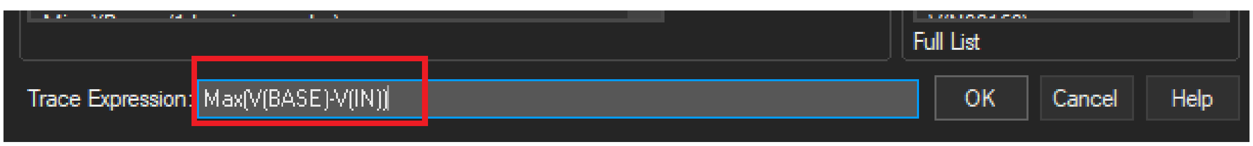


c. The cursor is moved outside of the parenthesis, but you are not done with this expression. Press the <u>left arrow on your keyboard once</u> to put the cursor back inside the right parenthesis.

d. Press the **minus (-)** key on your keyboard.

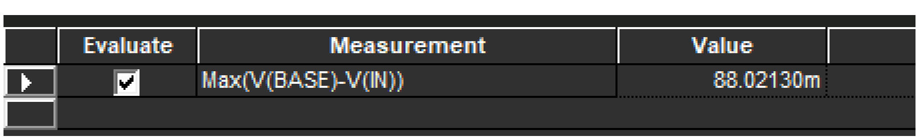


e. Left-click on **V(in)**.



The expression at the bottom of the form should now read **Max(V(base)-V(in))**. If it does not read so, edit it until it does, or clear the text and start over.

71. Select **OK** in the **Evaluate Measurement** form. The expression and its result are now displayed below the waveforms in the Probe window. The results compare favorably with the manually measured value.



	Evaluate	Measurement	Value
▶	☑	Max(V(BASE)-V(IN))	88.02130m

Figure 2-44: Measurement and its Result

72. Left-click on the line below the measurement result to reinvoke the Evaluate Measurement from. You will now create the second measurement.

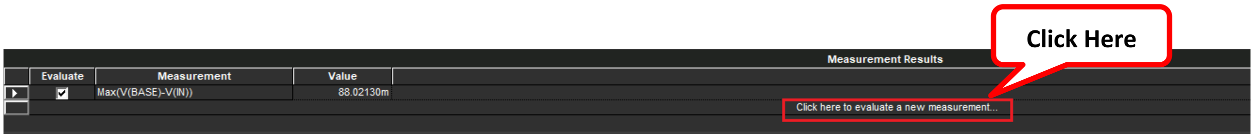


Figure 2-45: Adding a new measurement

73. For expedience, cut/paste the expression for the next measurement into the **Trace Expression** field. This measurement will determine the point in time that the first measurement result occurs, that is, the time that the maximum occurs. Perform the following step:

   Type or copy/paste the expression given below into the **Trace Expression** field. If you are reading from a paper copy, you can find **`Measurements.txt`** in the **module2** folder. You can open it with a text editor or by using the Probe menu item **File > Open** (filter set to .txt) as a copy/paste source.

   Expression: **`XatNthY((V(base)-V(in)-Max(V(base)-V(in))*.999999),0,1)`**

74. Select **OK** in the Evaluate Measurement form. The expression and its result are now displayed below the waveforms in the Probe window. The results in Figure 2-46 compare favorably with the manually measured value as well as the event time identified by the assertion. The measurement result below does not match the assertion result exactly. This is because the measurement is produced from the waveform results, which include interpolation between data points, while the assertion conditions are evaluated only at discrete time steps.

	Evaluate	Measurement	Value
	☑	Max(V(BASE)-V(IN))	88.02130m
▶	☑	XatNthY((V(base)-V(in)-Max(V(base...	109.12735u

Figure 2-46: Both Measurements

Note: If you are wondering what the .999999 in the second expression was for, read the description below; otherwise, skip ahead to step 75.

Review the entire measurement:

```
XatNthY((V(base)-V(in)-Max(V(base)-V(in))*.999999),0,1)
```

The newest expression reports the X-axis (time) at which the underlined expression all-of-the-mumbo-jumbo-on-the-left (the underlined expression argument to the XatNthY function) exceeds zero (the "0" argument) for the first time (the "1" on the right – there should only be one occurrence with the numeric precision in use).

The expression can be broken into the following two portions:

1) **V(base)-V(in)**: This is the voltage difference at any given time.
2) **Max(V(base)-V(in))*.999999**: This is overall maximum voltage difference (essentially your first measurement)—a constant threshold that will have to be evaluated before the complete measurement result can be determined.

So, the measurement will report the time that the *actual* exceeds the *threshold*. Since (2) will be tangentially intersected by (1), it is conceivable that rounding errors in the math might cause the measurement not to work. Lowering the threshold by a miniscule amount (factor of .999999) will greatly increase the likelihood of success without a significant error in the results.

Lab 12: Bias Point Display

Bias point display allows the results of the bias point analysis, which is typically automatically run as a precursor to a time-domain simulation, to be displayed on the schematic. The bias point analysis is a steady-state analysis under time=0 conditions.

75. In Capture, select **PSpice > Bias Points > Enable Bias_Voltage Display**. This reads the bias point run results into Capture.

76. Select (checked) **PSpice > Bias Points > Enable**. This enables bias display buttons in the analog toolbar.

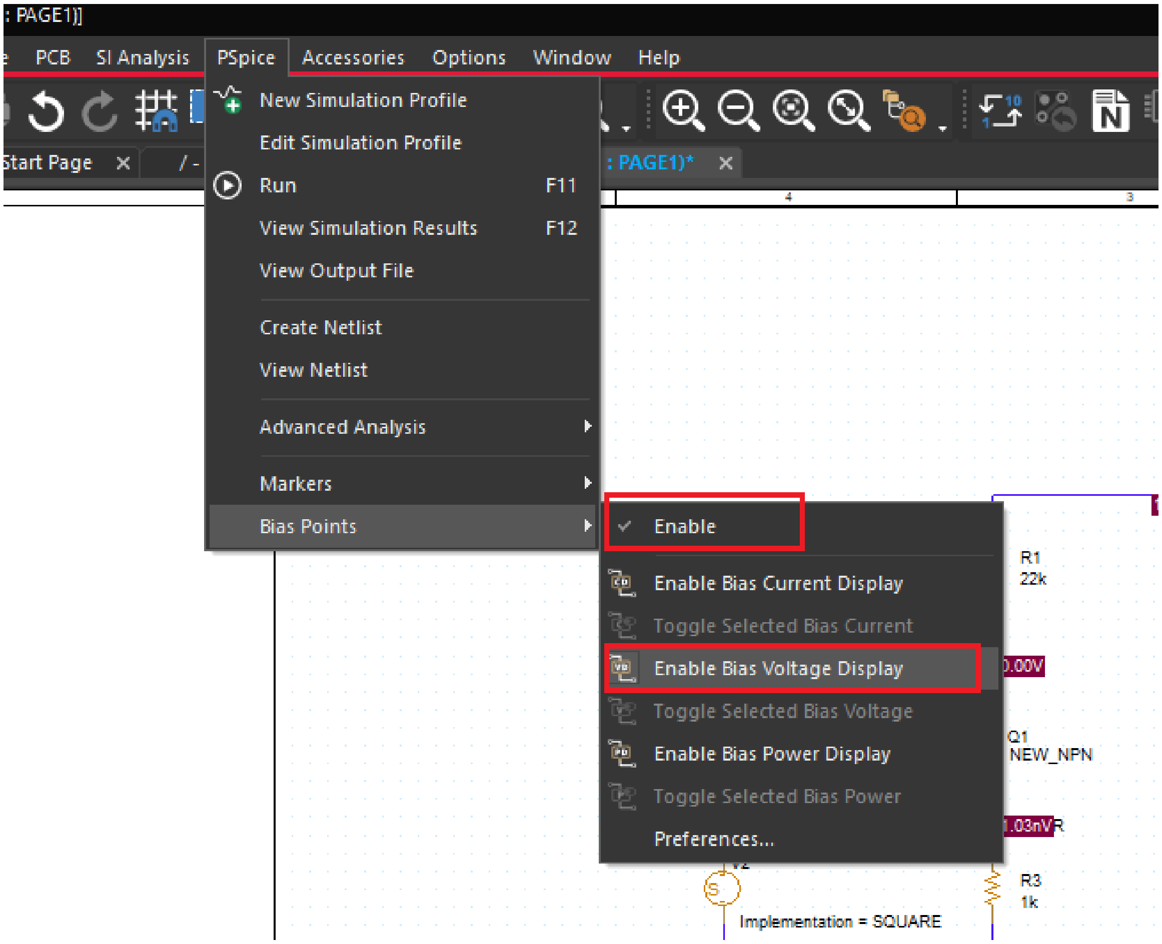


Figure 2-47: Enabling bias data on the schematic canvas

77. Cycle through the bias display buttons on the analog toolbar to view the bias data on the Capture canvas, as shown in Figure 2-48.

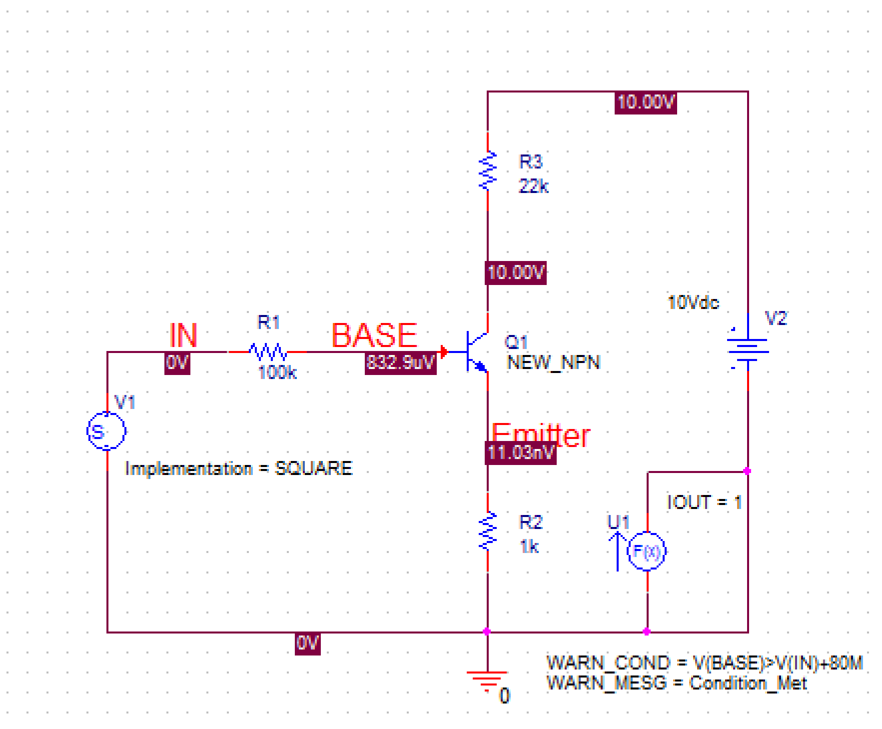


Figure 2-48: Bias Point display with Bias Voltage enabled

78. Disable the bias display using **PSpice > Bias Points > Enable** (unchecked) OR by toggling bias buttons in the analog toolbar.

79. Save the design.

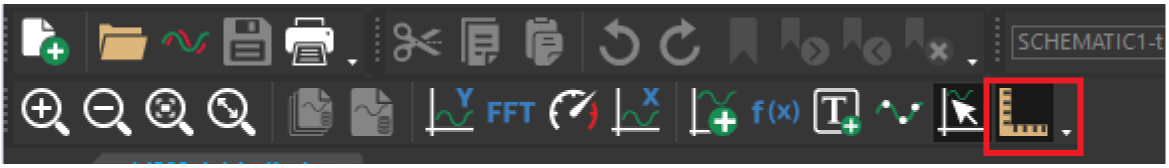
Lab 13: Restarting from a Saved Checkpoint

Earlier in this module, you enabled saving of simulation checkpoints at 100us intervals. Now, that a simulation has been completed, you have access to these checkpoints and can restart a simulation from one of these points. You will choose to restart from the 200us checkpoint.

80. Restore the Probe display to a suitable configuration by performing the following steps:

    a. If cursors are ON in **Probe**, turn them OFF by selecting the **Toggle Cursor** button.

b. Zoom to the entire waveform by selecting the **Zoom Fit** button.



c. Turn OFF the measurement display by deselecting **View > Measurement Results**.

81. Modify the simulation profile to restart the simulation from the 200us (simulation time) saved checkpoint by performing the following steps:

a. In **Capture**, select the **Edit Simulation Settings** analog toolbar button OR use **PSpice > Edit Simulation Profile**.

b. In the **Analysis** tab **> Options** section, uncheck the **Save Check Point** box and check the **Restart Simulation** box.

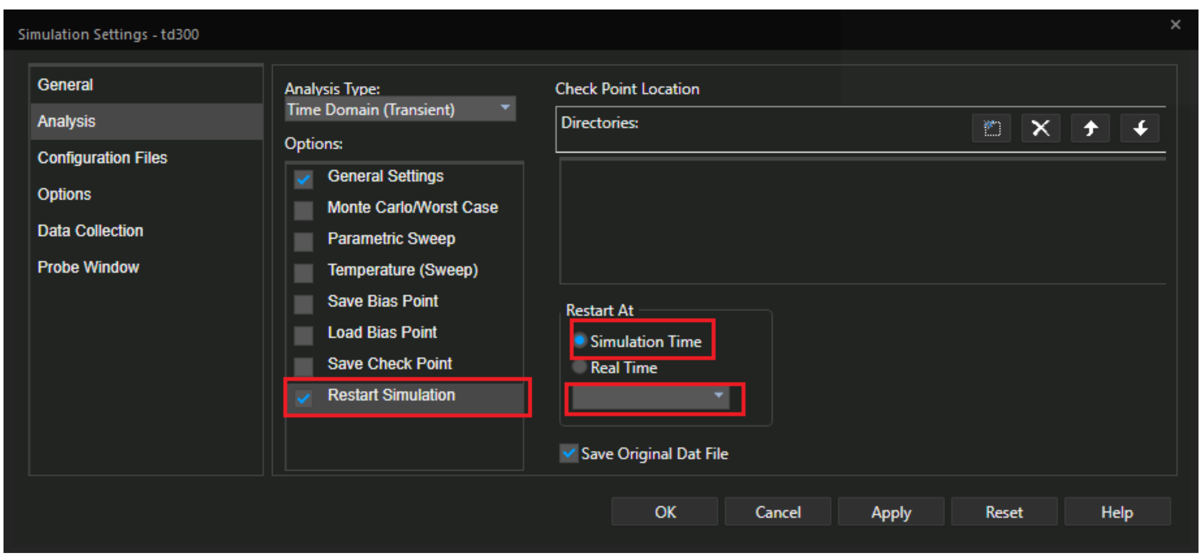


Figure 2-49: Setting Restart Point

c. In the **Restart At** section, select the pull-down value of **200.000us**.

d. Select **OK** in the Simulation Settings form.

82. Simulate the design (click ‘Yes’ to save). Simulation results in Figure 2-50 show the resulting waveforms ranging from the 200us check point to 300us.

As mentioned earlier, this is extremely useful when looking for an activity that takes place after a significant simulation time. After an initial complete simulation (with checkpoints saved), subsequent “restart” simulations can go much more quickly, and the simulation results files will generally be proportionately smaller. Another useful application for Checkpoint/Restart is in addressing convergence issues that could occur well into a long simulation run. In this case, you can make changes to component values and/or simulation settings to address the issue and then restart the simulation from the last saved checkpoint before the convergence error.

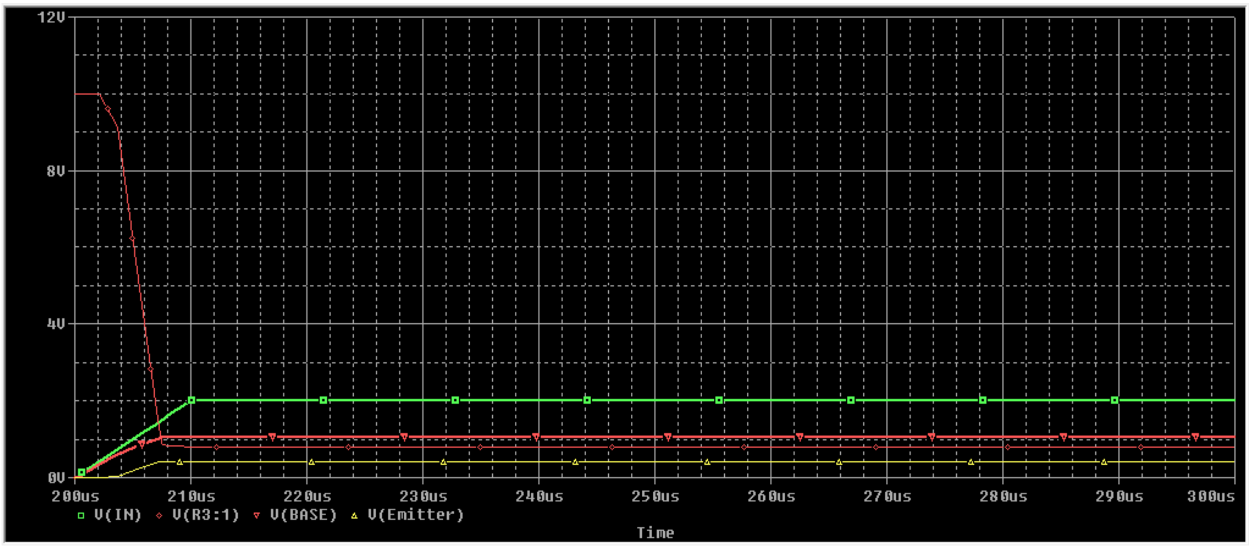


Figure 2-50: Simulation Restart Results from 200us

Based on the simulation results, measurements, and so on, you would be satisfied that your design functions as desired. You will now move to designs of increased complexity to perform more advanced simulations and analysis.

83. This completes Module 2. Close all windows/applications. No need to save.

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